PD - 94858

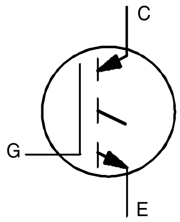
International
IOR Rectifier

IRG4PC50WPbF

INSULATED GATE BIPOLAR TRANSISTOR

Features

- Designed expressly for Switch-Mode Power Supply and PFC (power factor correction) applications
- Industry-benchmark switching losses improve efficiency of all power supply topologies
- 50% reduction of Eoff parameter
- Low IGBT conduction losses
- Latest-generation IGBT design and construction offers tighter parameters distribution, exceptional reliability
- Lead-Free



n-channel

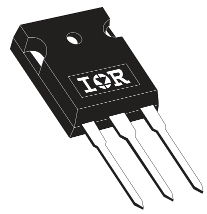
V_{CES} = 600V

$V_{CE(on)\ max.}$ = 2.30V

@V_{GE} = 15V, I_C = 27A

Benefits

- Lower switching losses allow more cost-effective operation than power MOSFETs up to 150 kHz ("hard switched" mode)
- Of particular benefit to single-ended converters and boost PFC topologies 150W and higher
- Low conduction losses and minimal minority-carrier recombination make these an excellent option for resonant mode switching as well (up to >300 kHz)



TO-247AC

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{CES}	Collector-to-Emitter Breakdown Voltage	600	V
I_C @ T_C = 25°C	Continuous Collector Current	55	A
I_C @ T_C = 100°C	Continuous Collector Current	27	
I_{CM}	Pulsed Collector Current ①	220	
I_{LM}	Clamped Inductive Load Current ②	220	
V_{GE}	Gate-to-Emitter Voltage	± 20	V
E_{ARV}	Reverse Voltage Avalanche Energy ③	170	mJ
P_D @ T_C = 25°C	Maximum Power Dissipation	200	W
P_D @ T_C = 100°C	Maximum Power Dissipation	78	
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds	300 (0.063 in. (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	–––	0.64	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	–––	
$R_{\theta JA}$	Junction-to-Ambient, typical socket mount	–––	40	
Wt	Weight	6 (0.21)	–––	g (oz)

11/26/03

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)CES}$	Collector-to-Emitter Breakdown Voltage	600	—	—	V	V_{GE} = 0V, I_C = 250µA
$V_{(BR)CES}$	Emitter-to-Collector Breakdown Voltage ④	18	—	—	V	V_{GE} = 0V, I_C = 1.0A
$\Delta V_{(BR)CES}/\Delta T_J$	Temperature Coeff. of Breakdown Voltage	—	0.41	—	V/°C	V_{GE} = 0V, I_C = 5.0mA
$V_{CE(ON)}$	Collector-to-Emitter Saturation Voltage	—	1.93	2.3	V	I_C = 27A; V_{GE} = 15V
		—	2.25	—		I_C = 55A; See Fig.2, 5
		—	1.71	—		I_C = 27A , T_J = 150°C
$V_{GE(th)}$	Gate Threshold Voltage	3.0	—	6.0		V_{CE} = V_{GE}, I_C = 250µA
$\Delta V_{GE(th)}/\Delta T_J$	Temperature Coeff. of Threshold Voltage	—	-11	—	mV/°C	V_{CE} = V_{GE}, I_C = 1.0mA
g_{fe}	Forward Transconductance ⑤	27	41	—	S	V_{CE} = 100 V, I_C = 27A
I_{CES}	Zero Gate Voltage Collector Current	—	—	250	µA	V_{GE} = 0V, V_{CE} = 600V
		—	—	2.0		V_{GE} = 0V, V_{CE} = 10V, T_J = 25°C
		—	—	5000		V_{GE} = 0V, V_{CE} = 600V, T_J = 150°C
I_{GES}	Gate-to-Emitter Leakage Current	—	—	±100	nA	V_{GE} = ±20V

Switching Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge (turn-on)	—	180	270	nC	I_C = 27A
Q_{ge}	Gate - Emitter Charge (turn-on)	—	24	36		V_{CC} = 400V See Fig.8
Q_{gc}	Gate - Collector Charge (turn-on)	—	63	95		V_{GE} = 15V
$t_{d(on)}$	Turn-On Delay Time	—	46	—	ns	
t_r	Rise Time	—	33	—		T_J = 25°C
$t_{d(off)}$	Turn-Off Delay Time	—	120	180		I_C = 27A, V_{CC} = 480V
t_f	Fall Time	—	57	86		V_{GE} = 15V, R_G = 5.0Ω
E_{on}	Turn-On Switching Loss	—	0.08	—	mJ	Energy losses include "tail"
E_{off}	Turn-Off Switching Loss	—	0.32	—		See Fig. 9, 10, 14
E_{ts}	Total Switching Loss	—	0.40	0.5		
$t_{d(on)}$	Turn-On Delay Time	—	31	—	ns	T_J = 150°C,
t_r	Rise Time	—	43	—		I_C = 27A, V_{CC} = 480V
$t_{d(off)}$	Turn-Off Delay Time	—	210	—		V_{GE} = 15V, R_G = 5.0Ω
t_f	Fall Time	—	62	—		Energy losses include "tail"
E_{ts}	Total Switching Loss	—	1.14	—	mJ	See Fig. 10,11, 14
L_E	Internal Emitter Inductance	—	13	—	nH	Measured 5mm from package
C_{ies}	Input Capacitance	—	3700	—	pF	V_{GE} = 0V
C_{oes}	Output Capacitance	—	260	—		V_{CC} = 30V See Fig. 7
C_{res}	Reverse Transfer Capacitance	—	68	—		ƒ = 1.0MHz

Notes:

① Repetitive rating; V_{GE} = 20V, pulse width limited by max. junction temperature. (See fig. 13b)

② V_{CC} = 80%(V_{CES}), V_{GE} = 20V, L = 10µH, R_G = 5.0Ω, (See fig. 13a)

③ Repetitive rating; pulse width limited by maximum junction temperature.

④ Pulse width ≤ 80µs; duty factor ≤ 0.1%.

⑤ Pulse width 5.0µs, single shot.

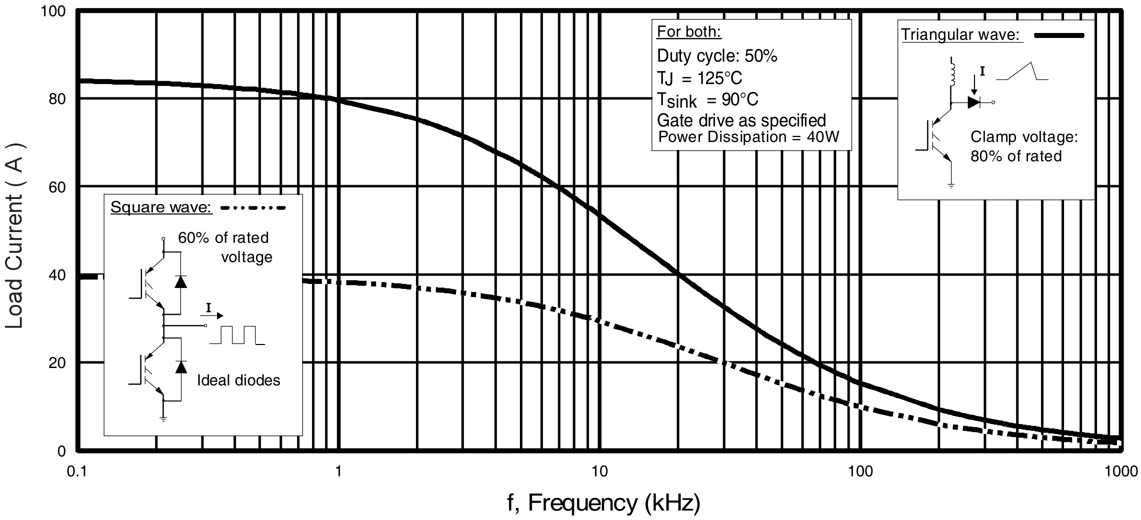


Fig. 1 - Typical Load Current vs. Frequency
(Load Current = I_{RMS} of fundamental)

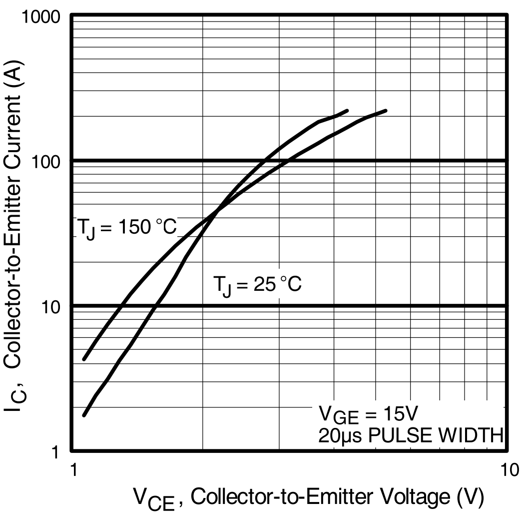


Fig. 2 - Typical Output Characteristics

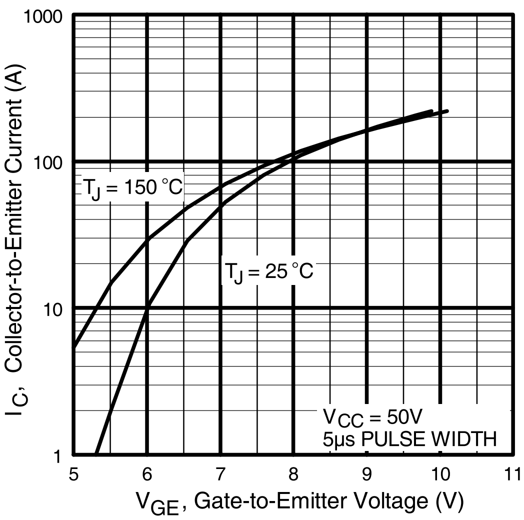


Fig. 3 - Typical Transfer Characteristics

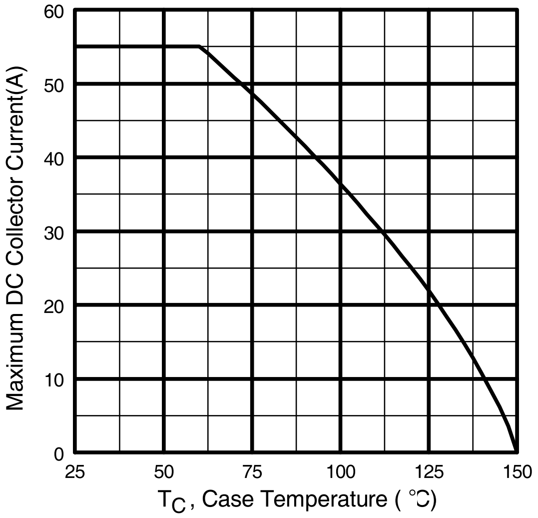


Fig. 4 - Maximum Collector Current vs. Case Temperature

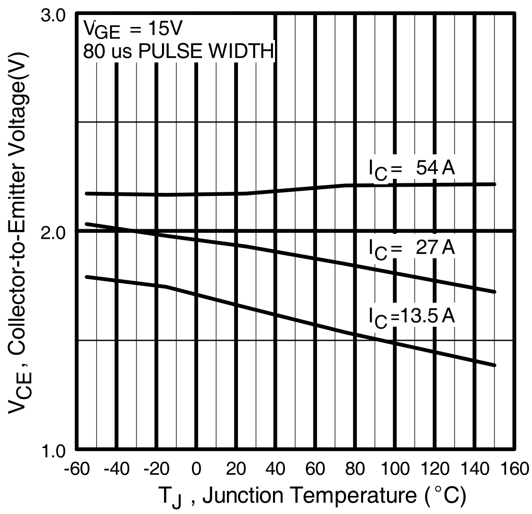


Fig. 5 - Typical Collector-to-Emitter Voltage vs. Junction Temperature

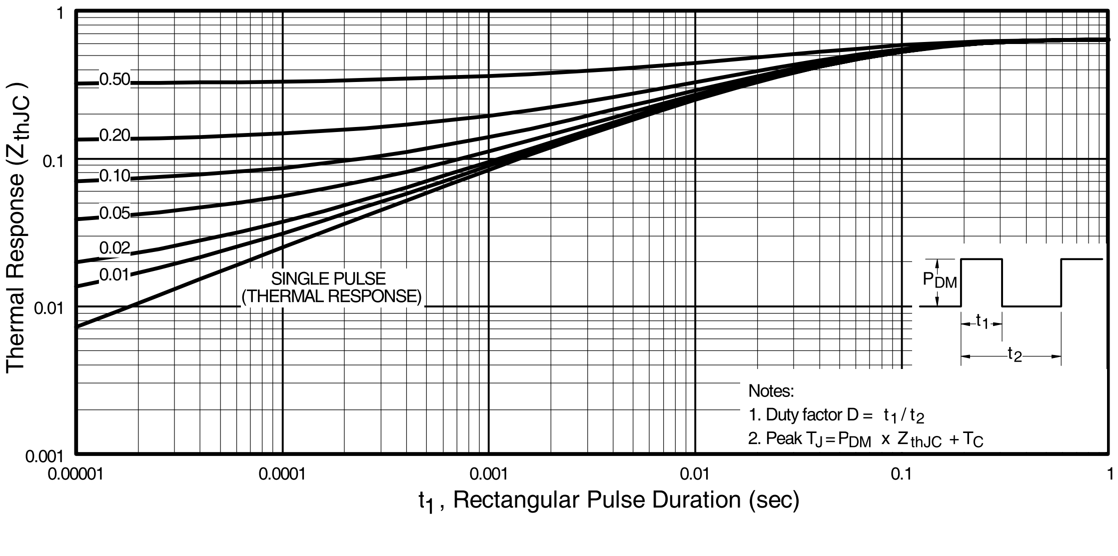


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

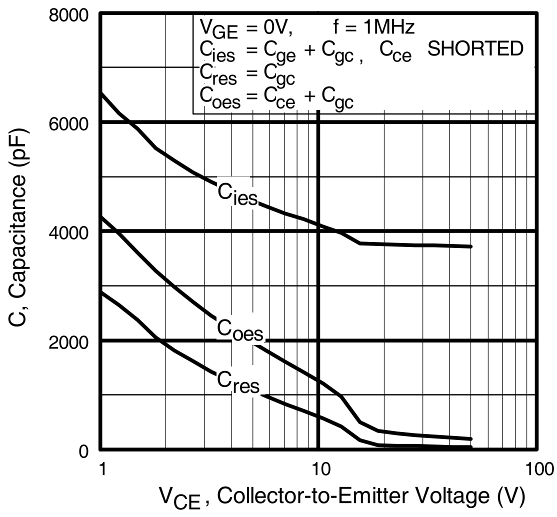


Fig. 7 - Typical Capacitance vs. Collector-to-Emitter Voltage

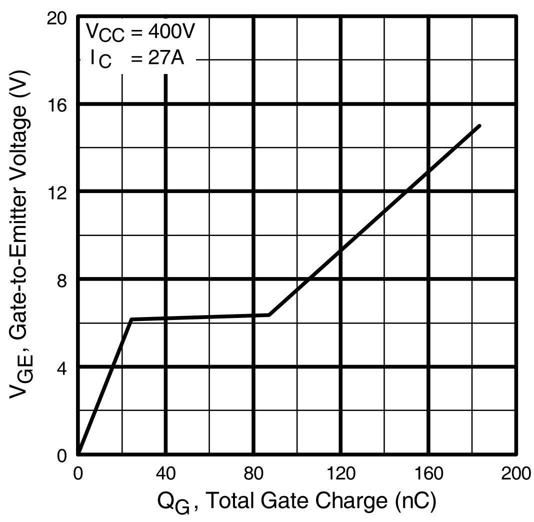


Fig. 8 - Typical Gate Charge vs. Gate-to-Emitter Voltage

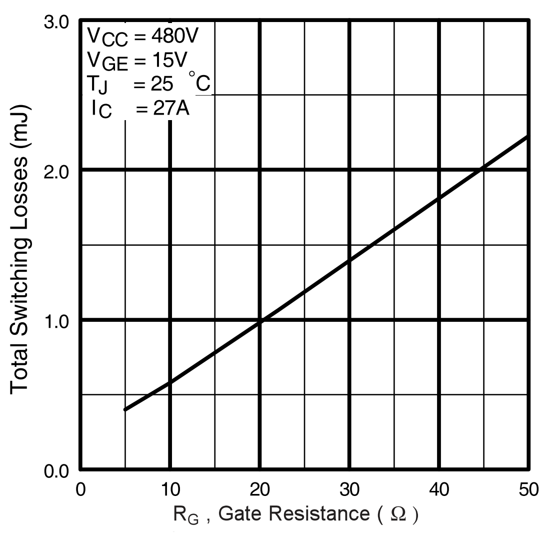


Fig. 9 - Typical Switching Losses vs. Gate Resistance

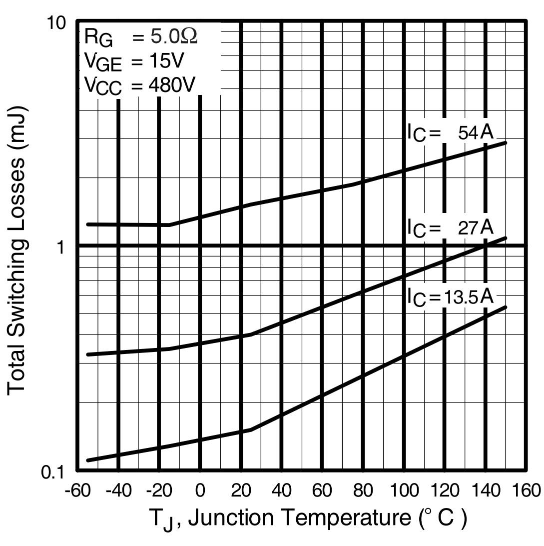


Fig. 10 - Typical Switching Losses vs. Junction Temperature

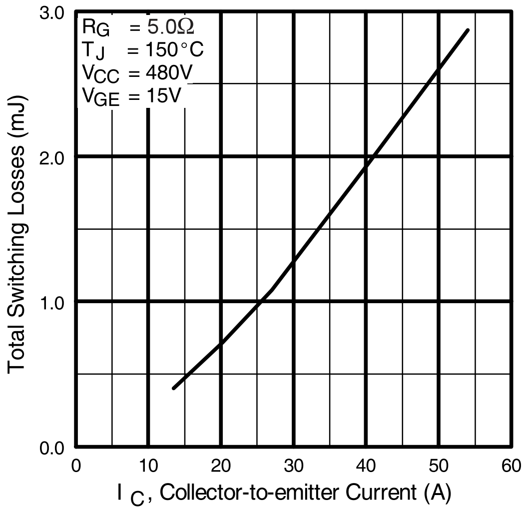


Fig. 11 - Typical Switching Losses vs. Collector-to-Emitter Current

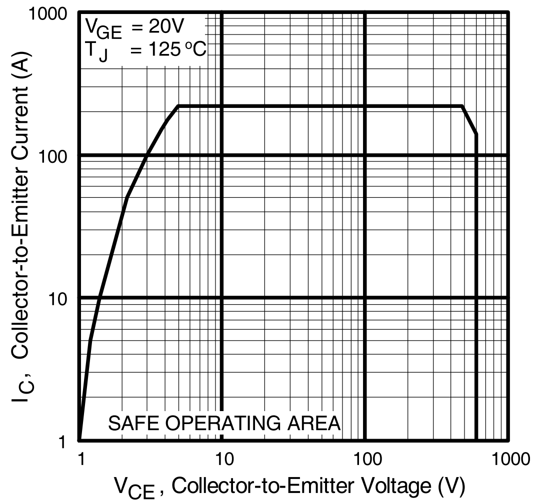


Fig. 12 - Turn-Off SOA

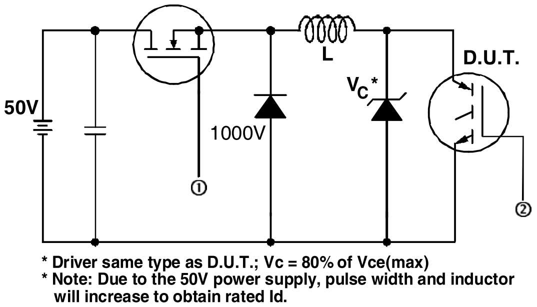


Fig. 13a - Clamped Inductive Load Test Circuit

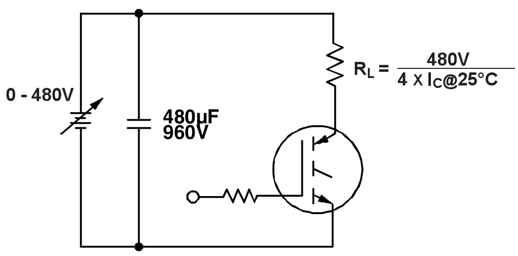


Fig. 13b - Pulsed Collector Current Test Circuit

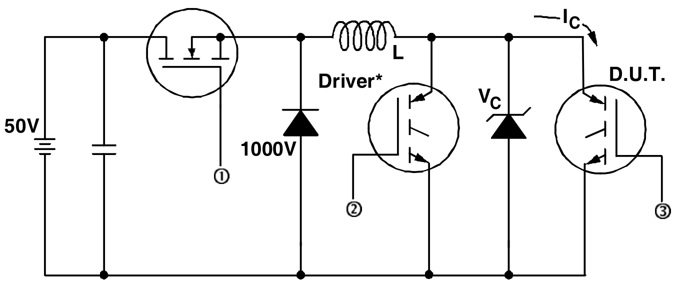


Fig. 14a - Switching Loss Test Circuit

* Driver same type as D.U.T., VC = 480V

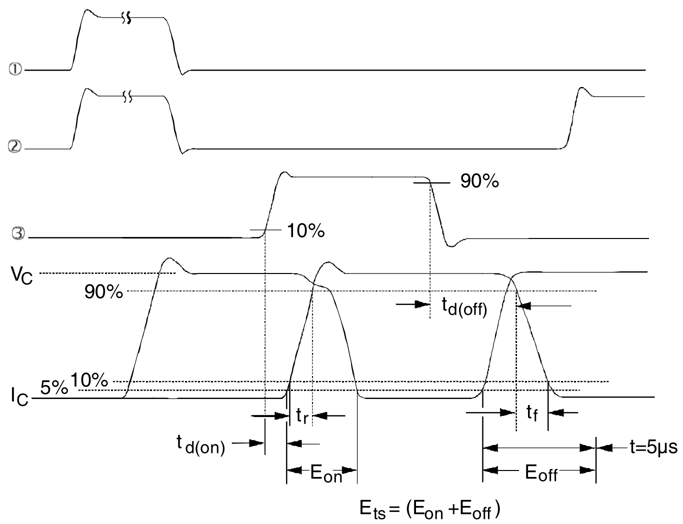
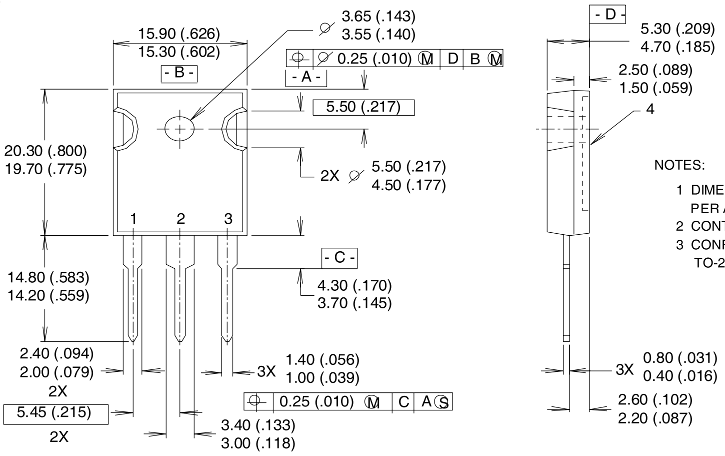


Fig. 14b - Switching Loss Waveforms

TO-247AC Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE TO-247-AC.

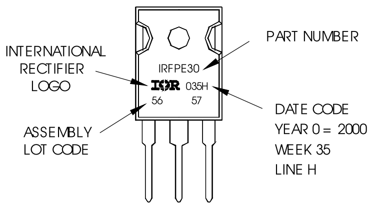
LEAD ASSIGNMENTS

Hexfet	IGBT
1 - Gate	1 - Gate
2 - Drain	2 - Collector
3 - Source	3 - Emitter
4 - Drain	4 - Collector

TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 5657
ASSEMBLED ON WW 35, 2000
IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.11/03

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/