SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

TEA2260/TEA2261 HIGH PERFORMANCE DRIVER CIRCUITS FOR S.M.P.S

SUMMARY **Page**

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I - INTRODUCTION

The TEA2260/61 is an integrated circuit able to drive a bipolar transistor directly with an output base current up to 1.2A.

So the TEA 2260/61 covers a wide range of application from 80W to more than 200W with all safety requirements respected.

The high performances of the regulation loop provide a very low output power due to an automatic burst mode.

The TEA2260/61 can be used in a MASTER SLAVE STRUCTURE, in a PRIMARY REGULATION or a SECONDARY REGULATION.

The TEA 2260/61 is very flexible and high performance device with a very large applications field.

The only difference between TEA2260 and TEA2261 concerns security functions (see paragraph II.8)

I.1 - Master Slave Mode (Figure 1)

In this configuration the master circuit located on the secondary side, generates PWM pulses used for output voltage regulation. These pulses are sent via a feedback transformer to the slave circuit (Figure 1).

In this mode of operation, the falling edge of the PWM Signal may be synchronized with an external signal. By this way the switching off time of the power transistor, which generates lot of parasites, can be synchronized on the line flyback signal in TV applications.

An other advantage of the MASTER SLAVE STRUCTURE is to have a very good regulation not depending of the coupling between transformer primary and secondary windings, which allows the use of low cost switch mode transformers.

I.2 - Burst Mode (Figure 2)

During start-up and stand-by phases, no regulation pulses are provided by the master circuit to the slave circuit.

The slave circuit operates in primary regulation mode. When the output power is very low the burst mode is automatically used.

This operating mode of the SMPS effectively provides a very low output power with a high efficiency.

The TEA2260/61 generates bursts with a period varying as a function of the output power.

Thus the output power in burst mode can varied in a wide range from 1W to more than 30W.

I.3 - Operation of Master Slave Power Supply in TV Application

The system architecture generally employed is depicted in Figure 3. On the secondary side a micro controller is connected to the remote control receiver which generates control signal for the stand-by and normal modes of operation (Figure 4).

- In stand-by mode, the device power consumption is very low (few watts). The master circuit does not send pulses and hence the slave circuit works in primary regulation and burst mode.
- In the normal mode, the master circuit provides the PWM signal required for regulation purposes. This is called MASTER SLAVE MODE. The master circuit can be simultaneously synchronized with the line flyback signal.
- Power supply start-up. As soon as the V_{CC}(start) threshold is reached, the slave circuit starts in continuous mode and primary regulation as long as the nominal output voltages are not reached. After this start-up phase the microcontroller holds the TV Set in stand-by mode or either in normal mode.

Figure 1

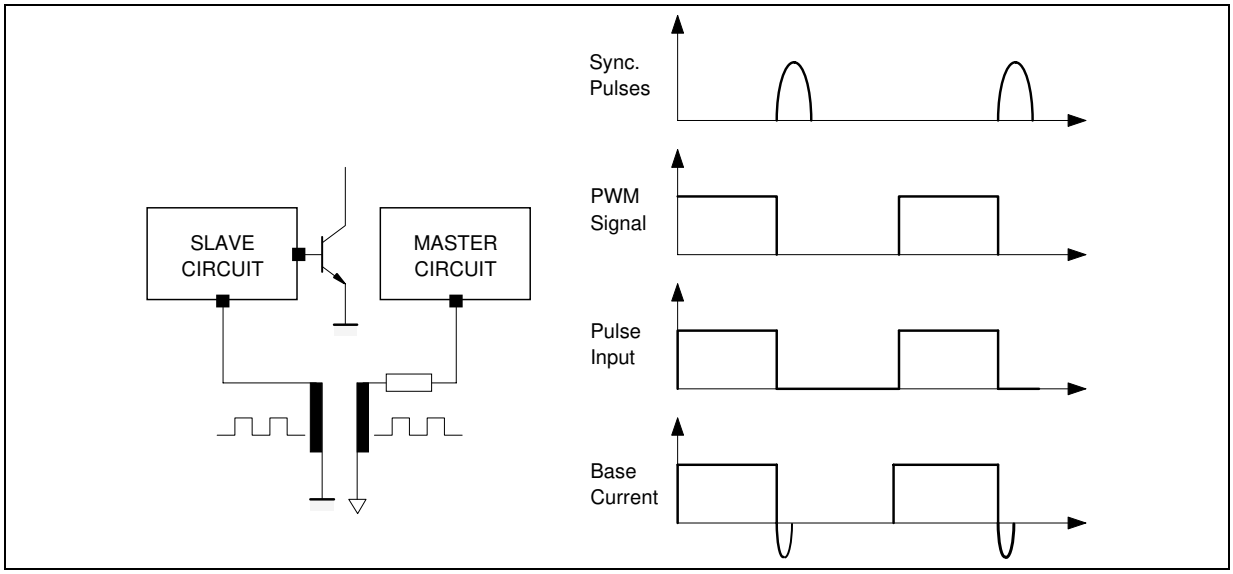


Figure 2 : Burst Mode Operation

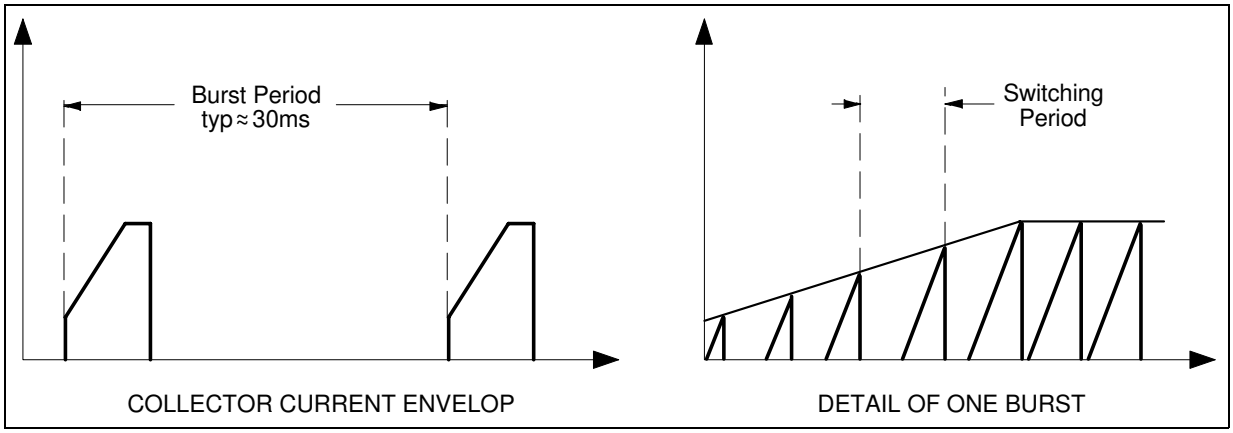


Figure 3 : TV Application System Diagram

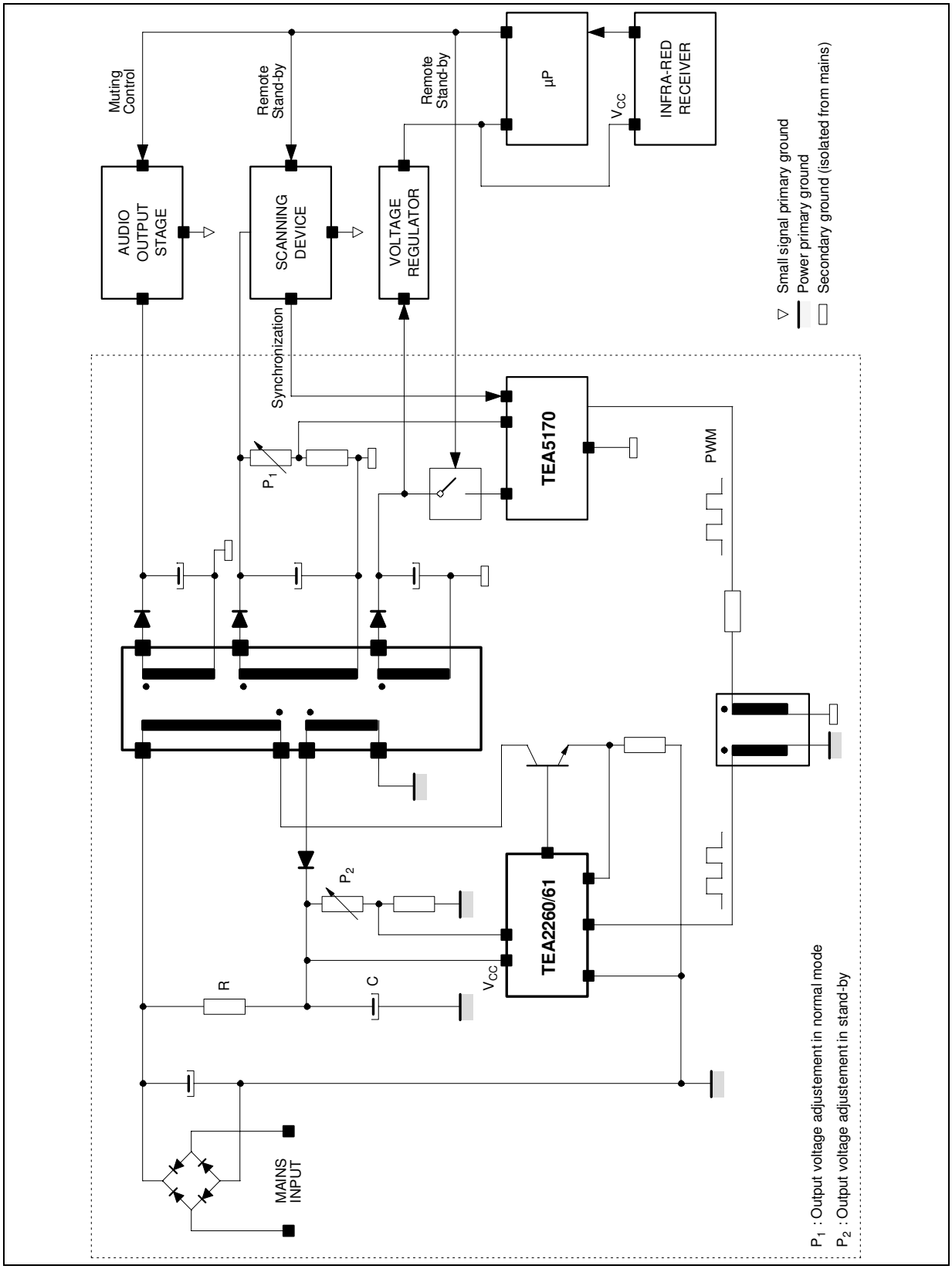
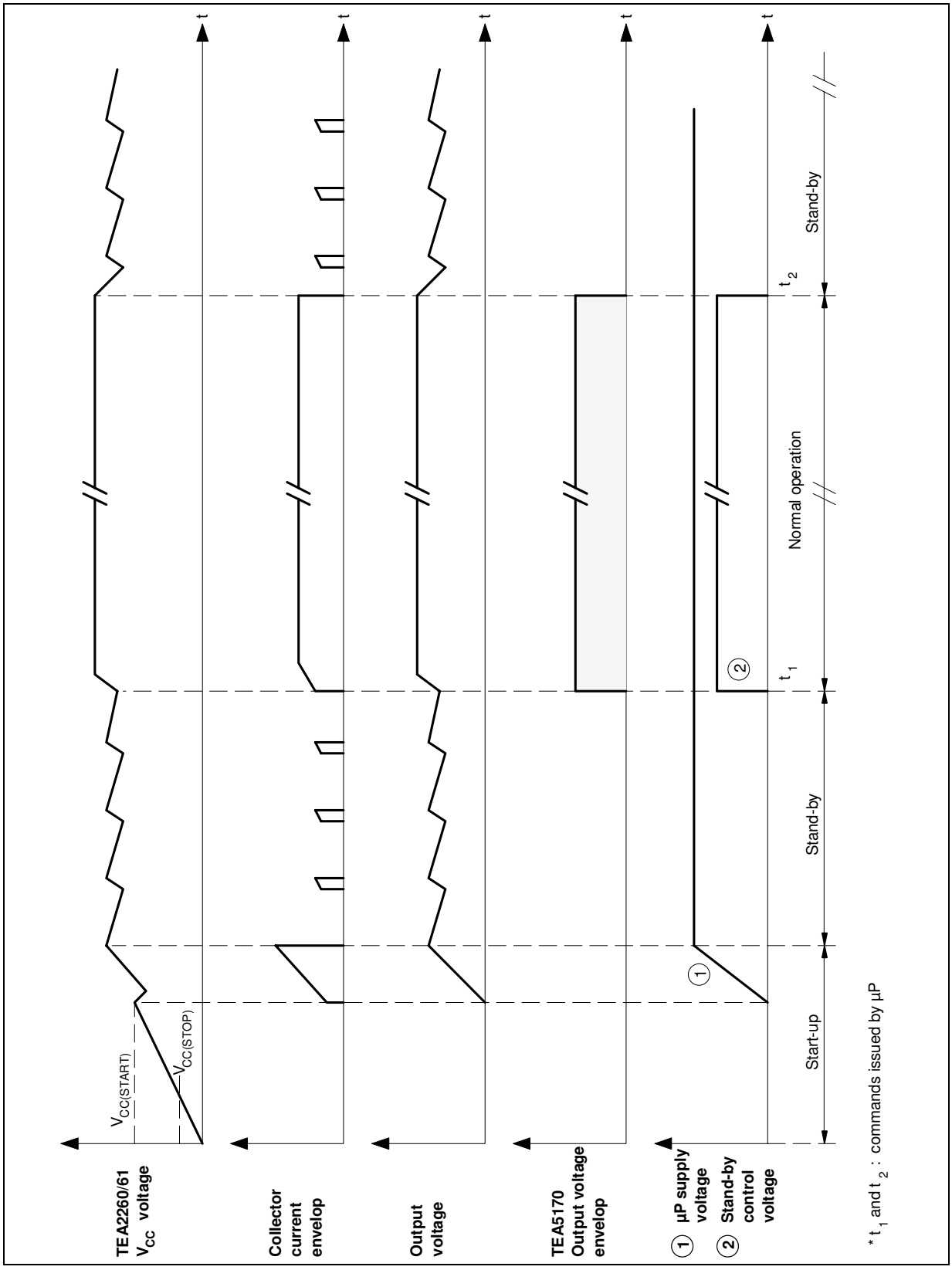


Figure 4 : System Description (waveforms)



I.4 - Secondary Regulation (Figures 5 and 6)

In this configuration the TEA2260/61 provides the regulation through an optocoupler to ensure good accuracy.

The advantage of this configuration is the avaibility of a large range of output power variation (e.g 1W to 110W).

This feature is due to the automatic burst mode (see paragraph II.6).

The structure in a TV Set is simpler than the MASTER SLAVE STRUCTURE because the power supply switches from normal mode to burst mode automatically as a function of the output power.

Figure 5 : TV Application System Diagram

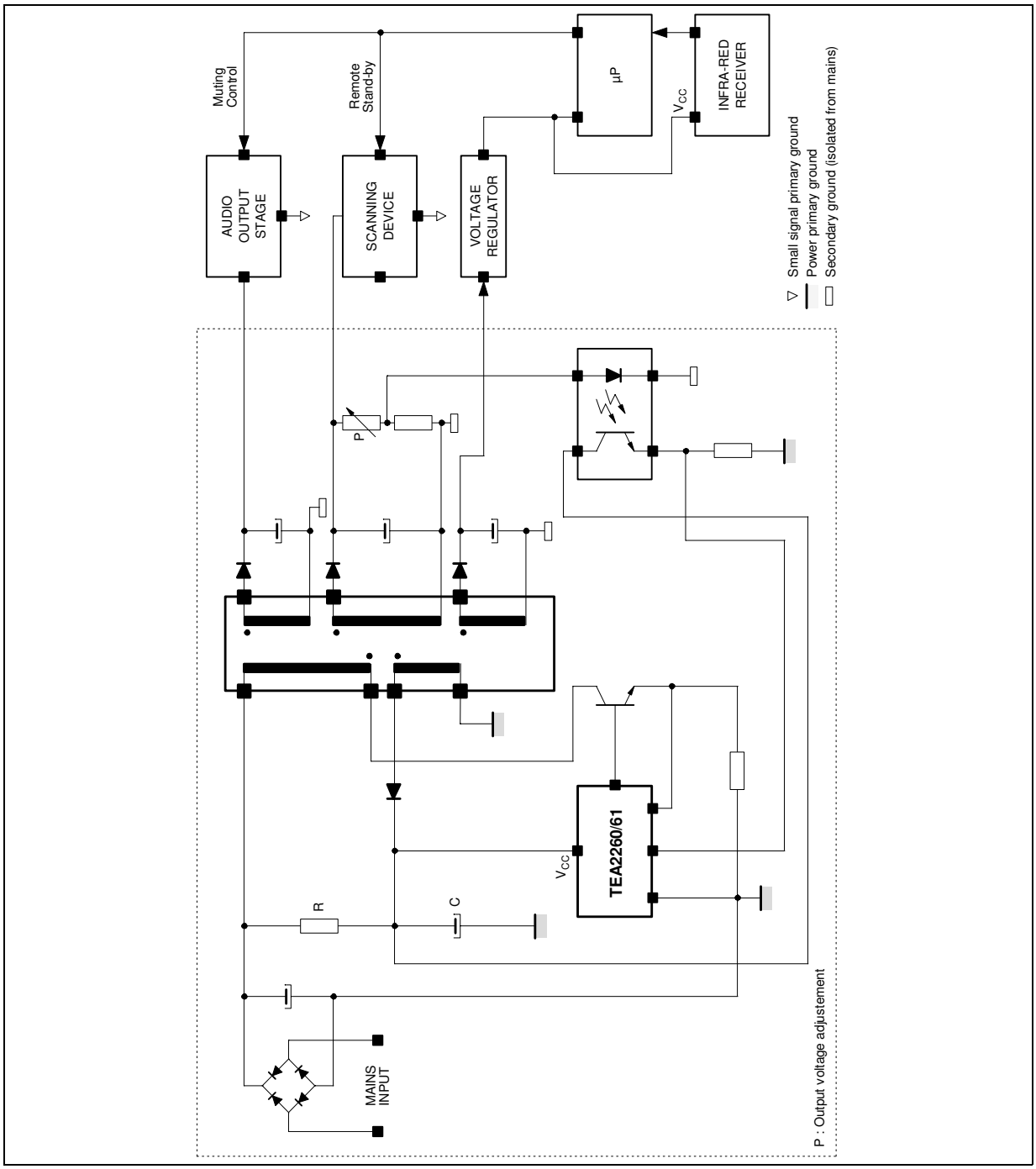
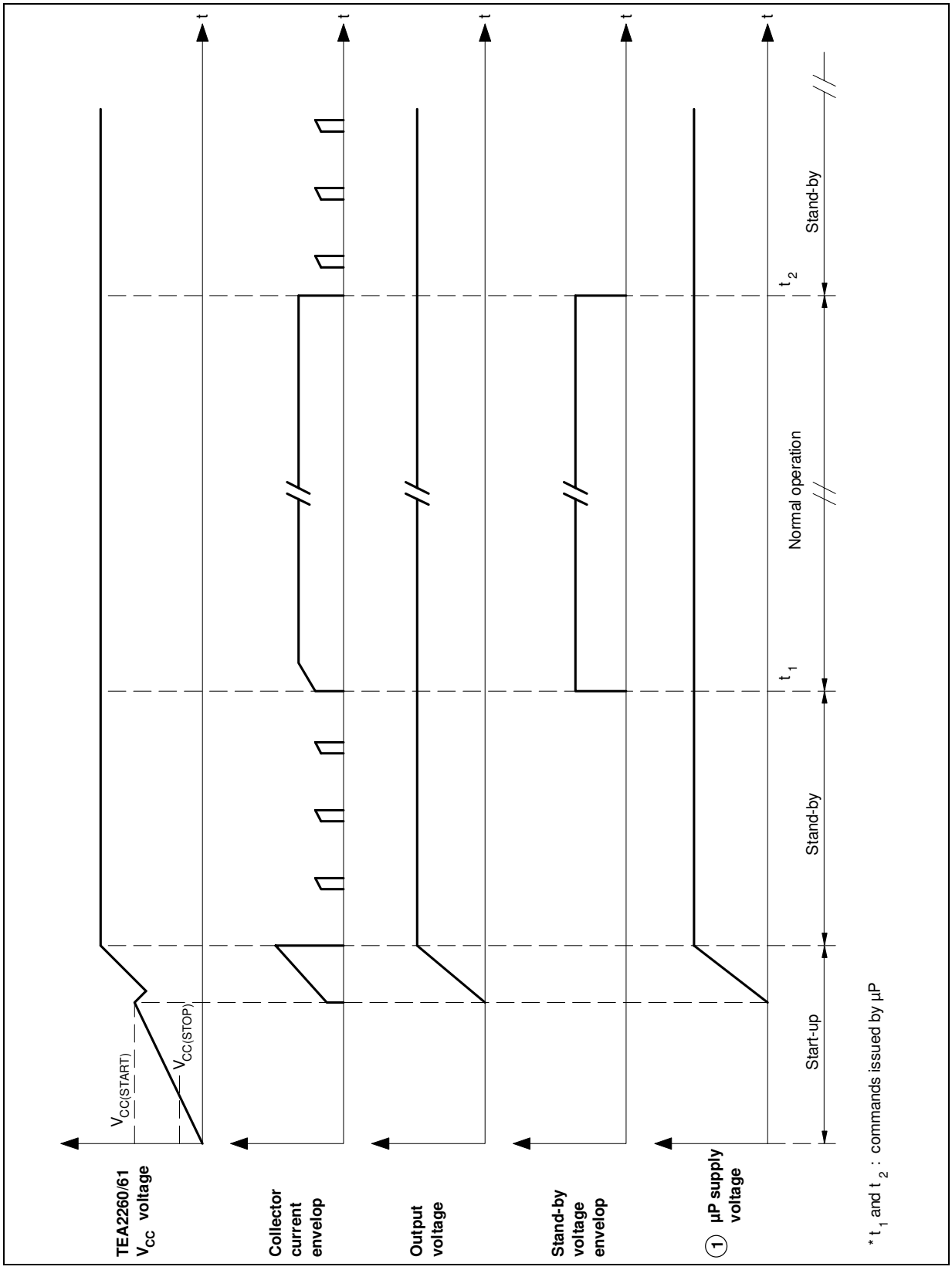


Figure 6 : System Description (waveforms)



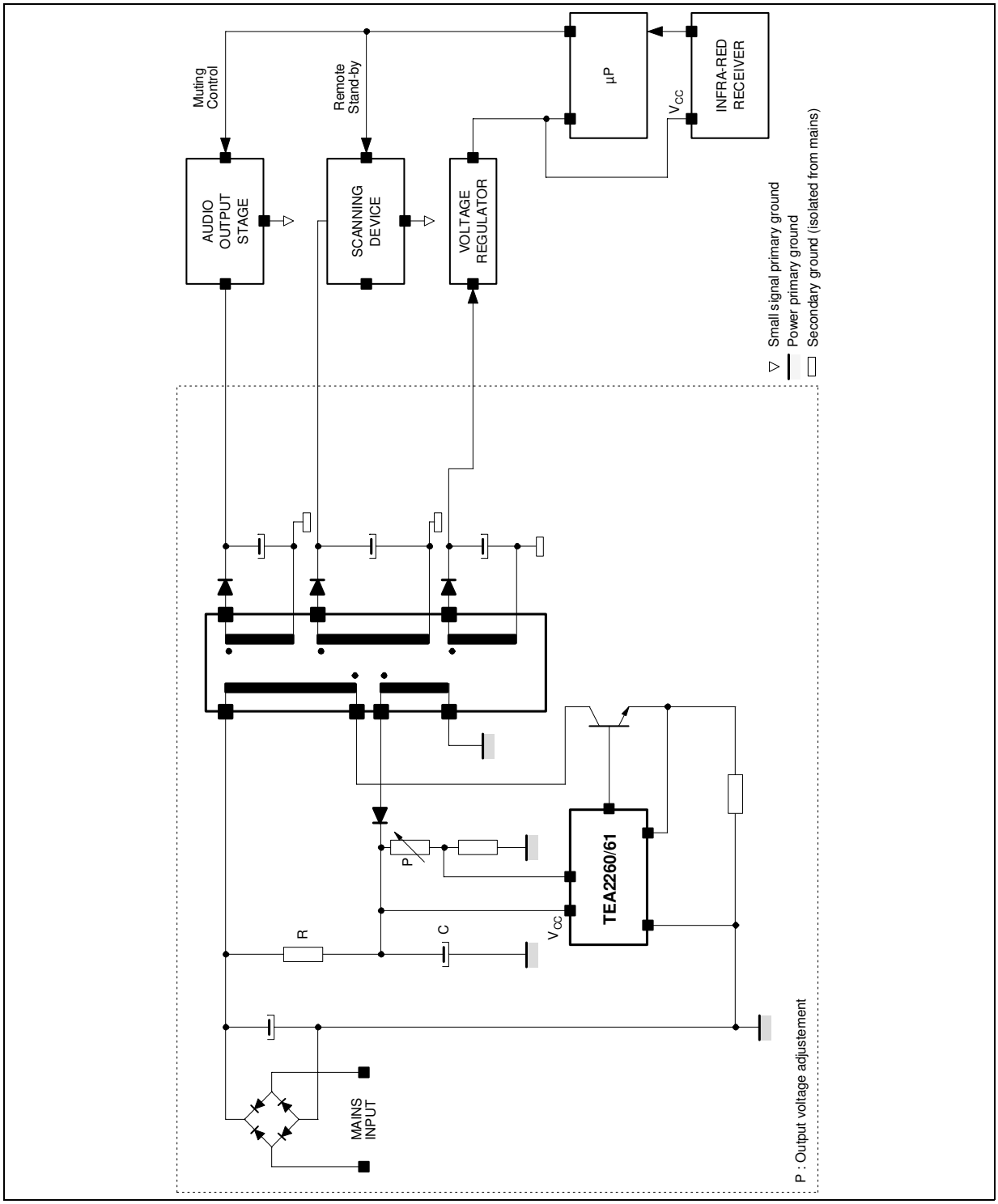
I.5 - Primary Regulation (Figure 7)

In this configuration the TEA2260/61 provides the regulation through an auxilliary winding.

This structure is very simple but the accuracy depends on the coupling between the transformer primary and secondary winding.

Due to the automatic burst mode the output power can vary in a large range.

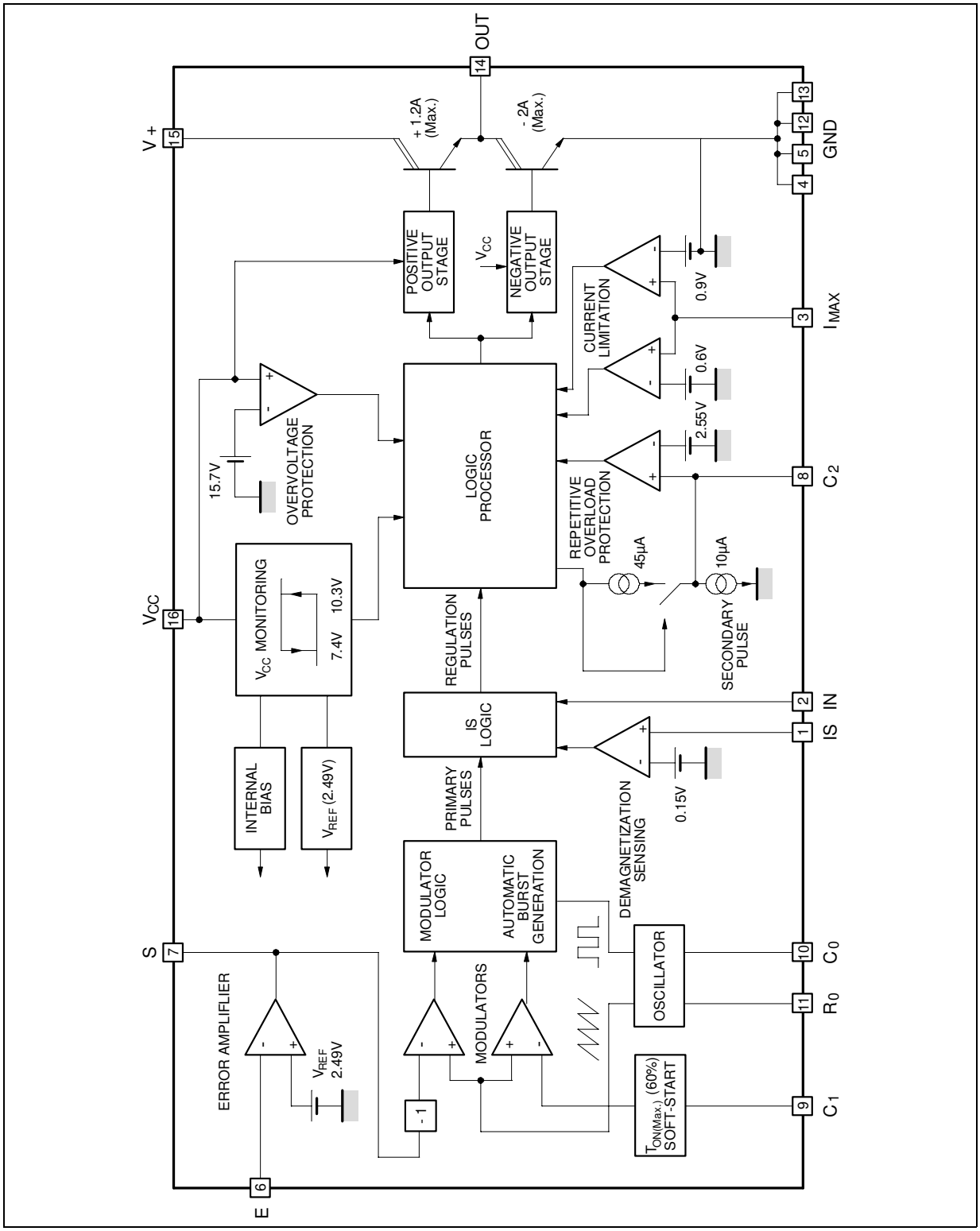
Figure 7 : TV Application System Diagram



II - CIRCUIT DESCRIPTION

Figure 8 shows the integrated functions.

Figure 8



The circuit contains 8 blocks :
- Voltage reference and internal V_{CC} generation.
- RC oscillator
- Error amplifier
- Pulse width modulator (PWM)
- "Is logic" for transformer demagnetization checking.
- Current limitation sub-unit (IMAX)
- Logical block.
- Output stage.

II.1 - Voltage Reference and Internal V_{CC} Generation (Figure 9)

This block generates a 2.5V typ. voltage reference valid as soon as V_{CC} exceeds 4V. It is not directly accessible externally but is transmitted to other blocks of the circuit.

This block also generates an internal regulated V_{CC}, $V_{CC(int)}$, the nominal value of which is 5V. $V_{CC(int)}$ supplies the circuit when Vcc is higher than $V_{CC(start)}$ (10.3V typ.).

This allows the circuit to achieve a good external V_{CC} rejection, and to provide high performance even with large V_{CC} supply voltage variations.

This block also generates initialization and control signals for the logical block. It also contains the $V_{CC(Max.)}$ comparator (typ threshold 15.7V).

II.2 - Oscillator (Figures 10 and 11)

The oscillator determines the switching frequency in primary regulation mode. Two external components are required : a resistor R_O and a capacitor C_O. The oscillator generates a sawtooth signal, which is available on Pin 10.

Figure 9 : Voltage Reference Block Principle

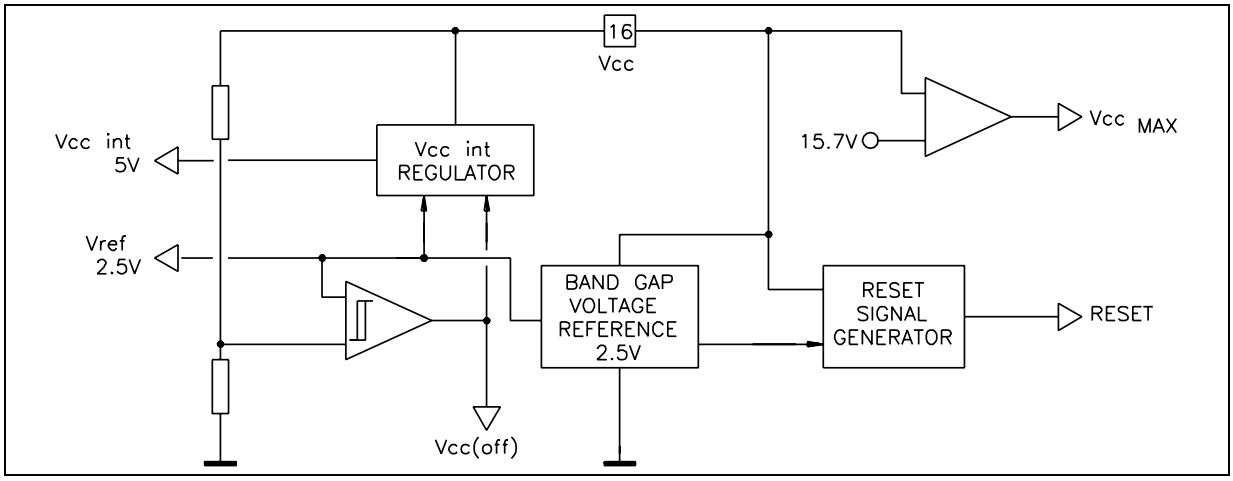


Figure 10 : Operating Principle

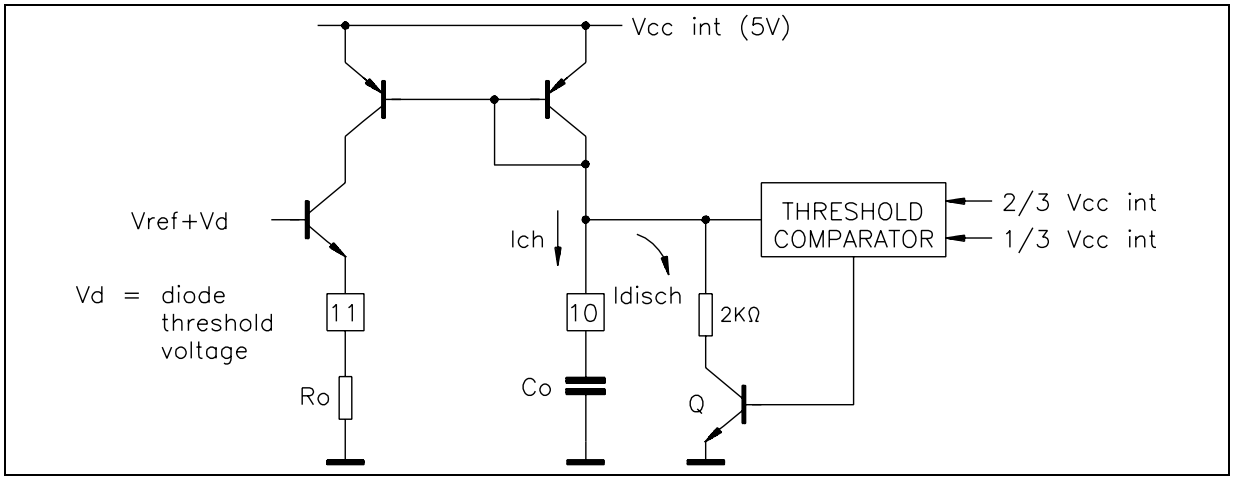
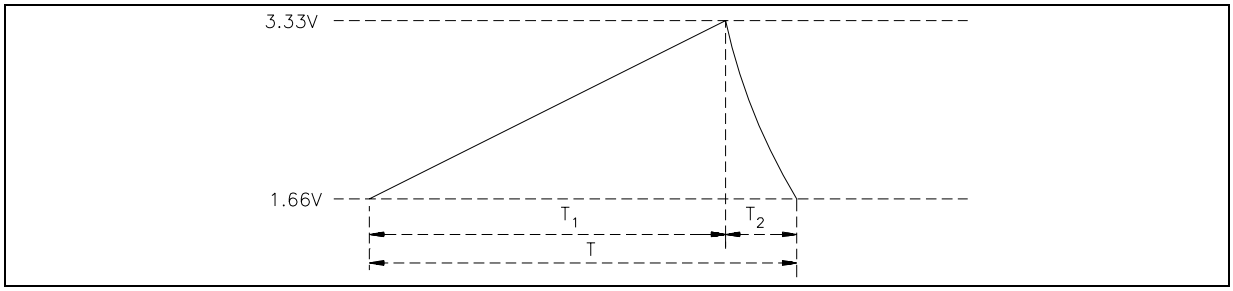


Figure 11 : Sawtooth available accross C_O



C_O capacitor is charged with a constant current. The current is fixed by R_O which is supplied by voltage V_{REF}.

$$I_{ch} = \frac{2.5}{R_O}$$

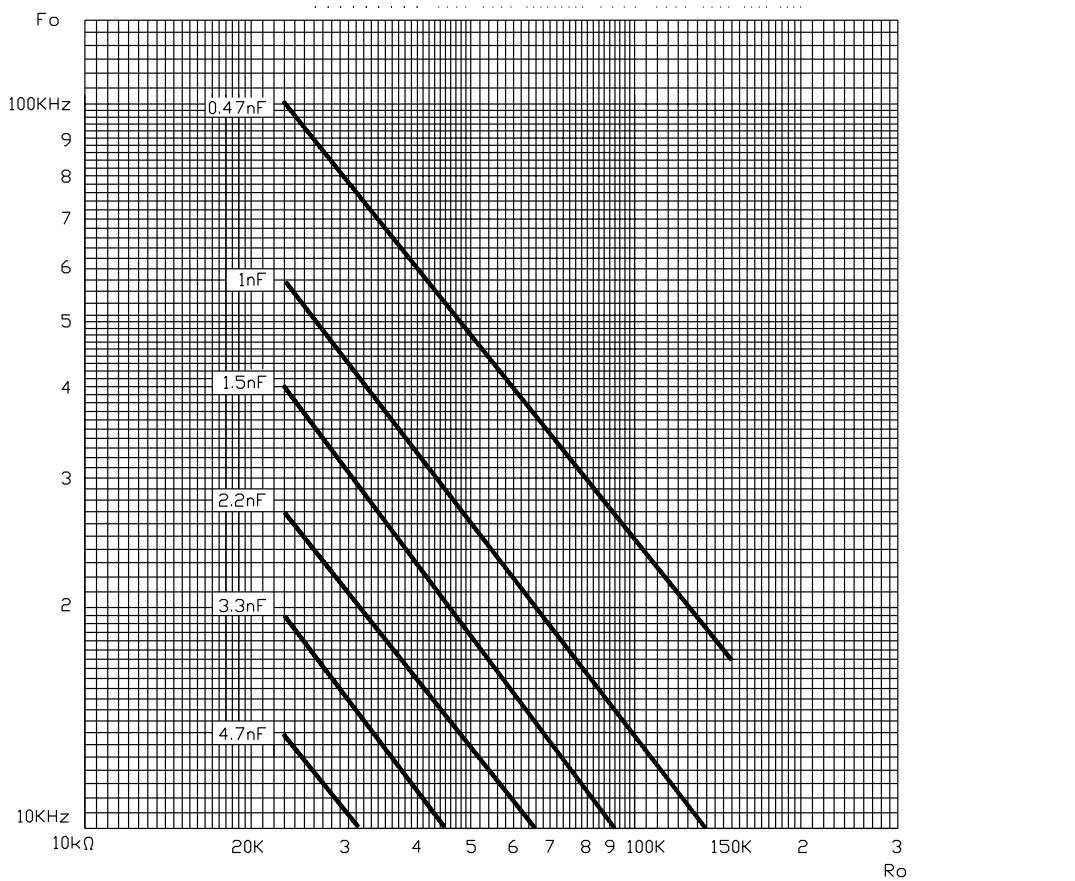
When the voltage across C_O reaches $\frac{2}{3}$ x V_{CCint} (typ 3.33V), Q Transistor conducts and C_O is quickly discharged into an 2kΩ (typ) internal resistor. When the voltage reaches 1/3 x V_{CCint} (typ 1.66V), the discharge is stopped, and the linear charge starts again.

Theoretical values of T,T_1 and T_2 as function of R_O and C_O :

$T = C_O$ (0.69 x R_O + 1380)
$T_1 = R_O$ x C_O x 0.69
$T_2 = C_O$ x 2000 x 0.69 = C_O x 1380

Due to the time response of comparators and normal spread on thresholds values, the real values of T_1 and T_2 may be slightly different, compared with these theoretical values (see Figure 12).

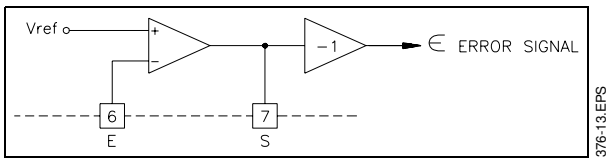
Figure 12 : Frequency as a Function of R_O and C_O



II.3 - Error Amplifier (Figure 13)

It is made of an operational amplifier. The open loop gain is typically 75dB. The unity gain frequency is 550kHz (typ). An internal protection limits the output current (Pin 7) at 2mA in case of shorted to ground.

Figure 13



Output and inverting input are accessible thus giving high flexibility in use. The non-inverting input is not accessible and is internally connected to V_{REF} (or $0.9V_{REF}$ in burst mode - see paragraph II.6)

Before driving the pulse width modulator (PWM) and in order to get the appropriate phase, the error amplifier is followed by an inverter.

II.4 - Pulse Width Modulator (PWM) (Figure 14)

The pulse width modulator consists of a comparator fed by the output signal of the error amplifier and the oscillator output. Its output is used to generate conduction signal.

The TEA2260/61 actually integrates two PWM :

- A main PWM generates a regulation signal ($\propto$) by comparing the error signal (inverted) and the sawtooth.
- An auxiliary PWM generates a maximum duty cycle conduction signal (β), by comparing the sawtooth with an internal fixed voltage. Furthermore, during the starting phase of the SMPS, in association with an external capacitor, this PWM generates increasing duty cycle, thus allowing a "soft" start-up.
- A logic "AND" between signals ($\propto$) and (β) provides the primary regulator output signal T_A.

Figure 14

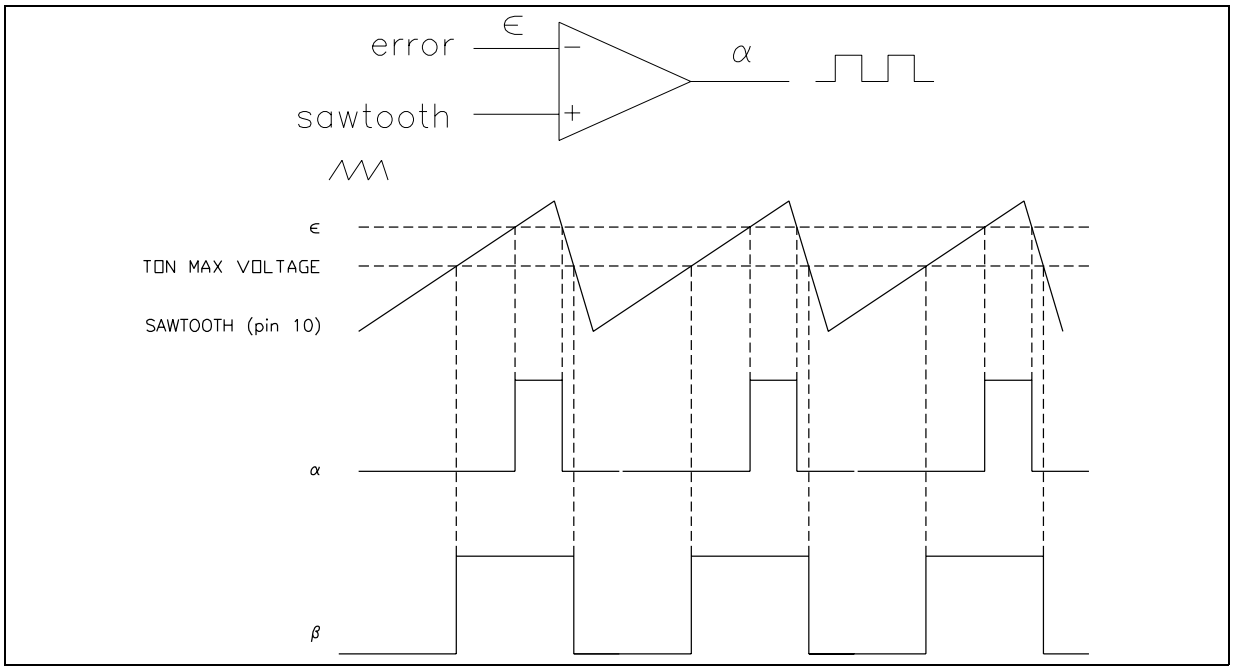
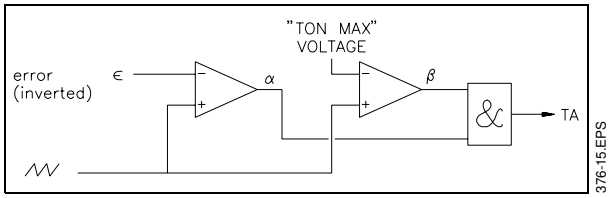


Figure 15



II.5 - Soft Start Operation (Figure 16)

From t_1 to t_2, there is no output pulse (pin 14) and C_1 is charged by a 180µA current (typically). When C_1 voltage reaches 1.5V (typically), output pulses appear and the charge current of C_1 is divided by 20 (9µA typically), then the duty cycle increases progressively. When C_1 voltage reaches 2.7V (typically), the soft-starting device ceases to limit the duty cycle, which may reach 60%.
Under established conditions C_1 voltage is charged to 3.1V (typically)

II.6 - Burst Generation in Stand By (primary regulation mode)

When the SMPS output power becomes very low, the duty cycle of the switching transistor conduction becomes also very low. In order to transmit a low average power, while ensuring correct switching conditions to the power transistor, a "burst" system is used for energy transmission in stand by mode.

Principle

For a medium output power (e.g. more than 10W), the voltage reference is applied to the non- inverting input of the error amplifier. When output power decreases as the minimum conducting time of the power transistor is reached, the output voltage tends to increase. Consequently the error signal applied to the PWM becomes higher than the sawtooth. This is detected by a special logic and the voltage applied to the non inverting input becomes V_{REF} = 0.9 x 2.5 = 2.25V typically.

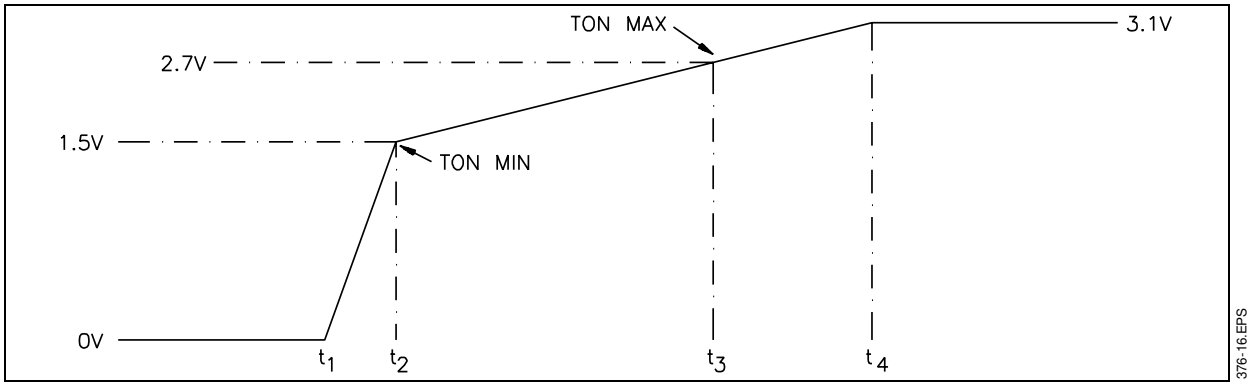
Consequently the regulation loop is in an overvoltage equivalent state and the output pulses disappear. The output voltage decreases and when it reaches a value near 0.9 times the normal regulation value , the voltage applied to the non inverting input is switched again to the normal value V_{REF} = 2.5V. Pulses applied to the power transistor reappear, the output voltage increases again, and so on... A relaxation operation is obtained, generating the burst.

Futhermore, to avoid a current peak at the beginning of each burst, the soft-start is used at this instant.

Advantages of this method

- improved power supply efficiency compared with traditional systems, for low power transmission.
- automatic burst-mode continuous mode transition, as a function of the output power.
- high stand-by power range.
- burst frequency and duty cycle adjustable with external components to the circuit.

Figure 16 : C1 Voltage (Pin 9)



II.7 - IS Logic (Figure 17)

During the transition from the "stand-by" mode to the "normal operating" mode, conduction pulses generated by the secondary regulator occur concurrently with those from the primary regulator.
These pulses are non-synchronous and this may be dangerous for the switching transistor. For example if the transistor is switched-on again during the overvoltage phase, just after switching-off, the FBSOA may not be respected and the transistor damaged.
To solve this problem a special arrangement checking the magnetization state of the power transformer is used.
The aim of the IS Logic is therefore to monitor the primary regulation pulses (TA) and the secondary regulation pulses (Pin 2), and to deliver a signal TB compatible with the power transistor safety requirements.

The IS Logic block comprises mainly two D flip-flops.

When a conduction signal arrives, the corresponding flip-flop is set in order to inhibit a conduction signal coming from the other regulation loop. Both flip-flops are reset by the negative edge of the signal applied to the demagnetization sensing input (Is Pin 1).

Note : The demagnetization checking device just described is only active when there are concurrently primary and secondary pulses, which in practice only occurs during the transient phase from Stand-by mode to normal mode.
When the power supply is in primary regulation mode **or** in secondary regulation mode, the demagnetization checking function is not activated.

Figure 17 : IS Logic Principle Schematic

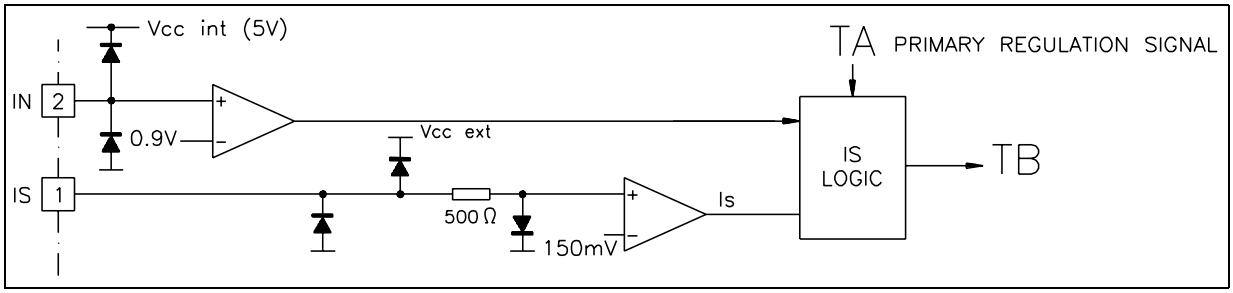
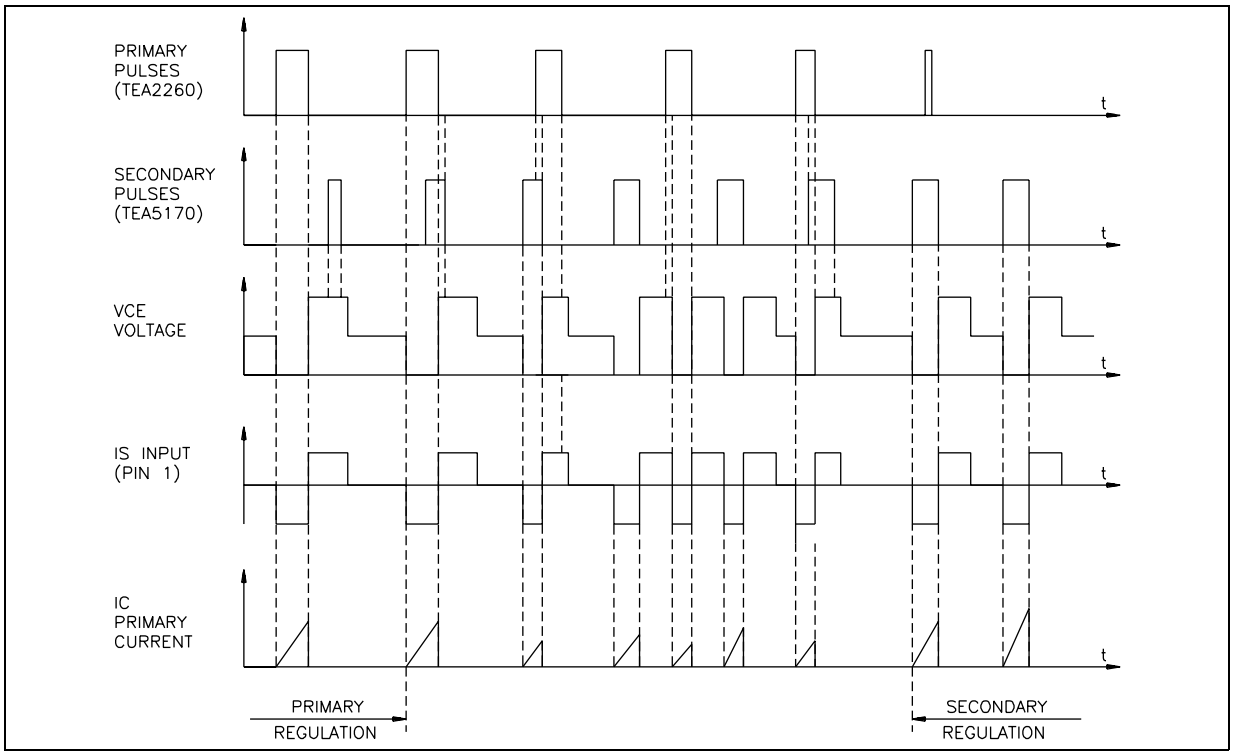


Figure 18



II.8 - Safety Functions :
Differences between TEA2260 and TEA2261

TEA2260

Concerning the safety functions, V_{CC}(max) (overvoltage detection) VIM1, VIM2 (overcurrent detection) the TEA2260 uses an internal counter which is incremented each time V_{CC}stop is reached (after fault detection) and try to restart. After 3 restarts with fault detection the power supply stops. But in certain cases where the TV set is supplied for a long time, without swich off, the power supply could stop (cases of tube flashes). In this case it is necessary to switch off the TV set and swich on again to reset the internal counter.

TEA2261

The safety detections are similar to TEA2260 for V_{CC}(max) (overvoltage detection) VIM1, VIM2 (overcurrent detection), but each time a fault detection is operating the C_2 capacitor is loaded step by step up to 2.6V, (case of long duration fault detection) and the power supply stpos. To discharge C_2 capacitor it is necessary to switch off the TV set and to switch on again and the power supply starts up.

Figure 19 : TEA2260 Safety Functions Flowchart

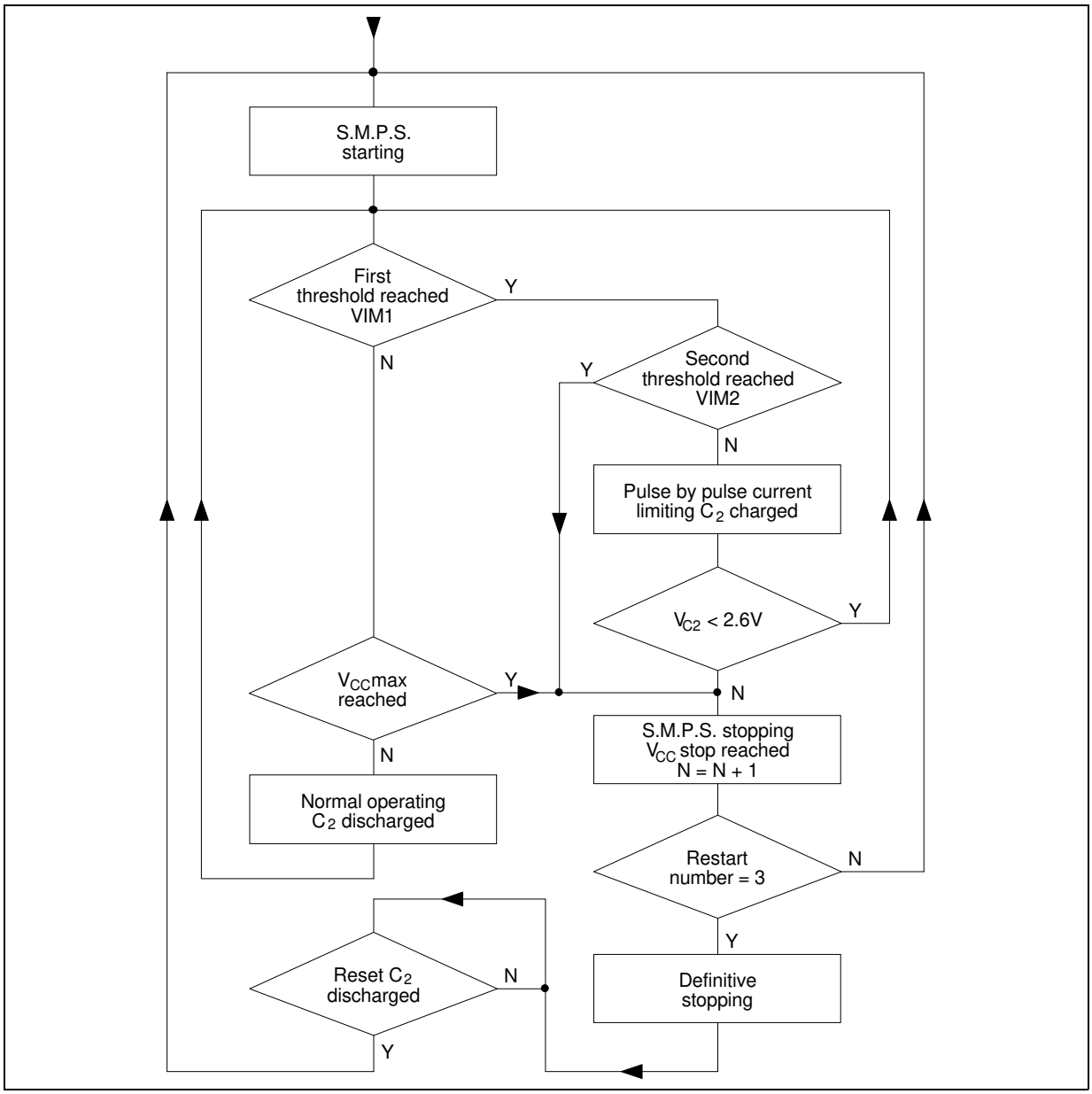
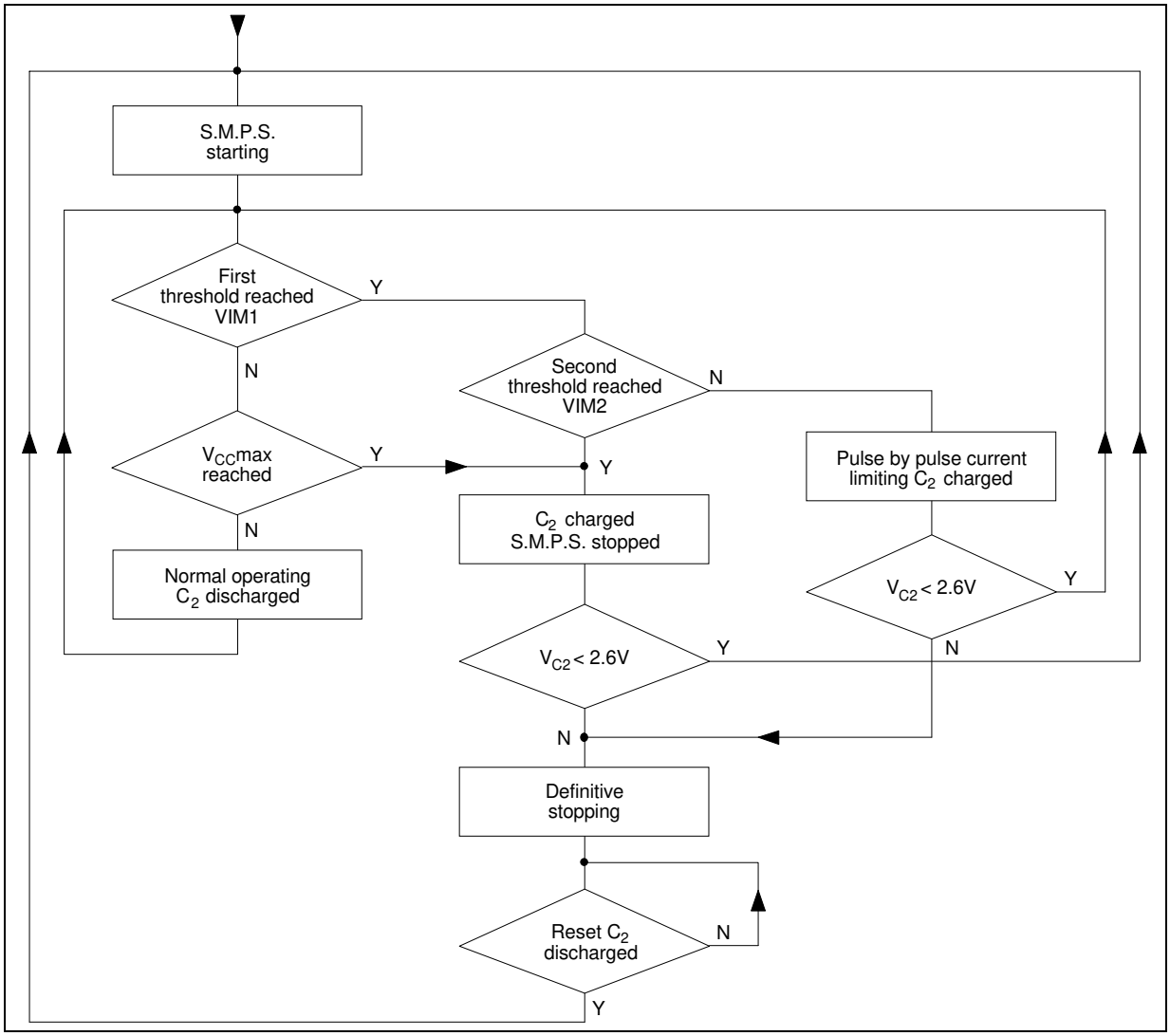


Figure 20 : TEA2261 Safety Functions Flowchart

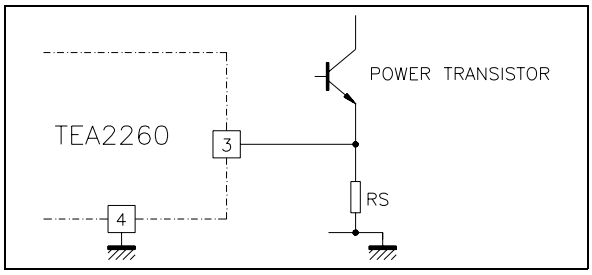


II.8.1. I Max (power transistor current limitation)

The current is measured by means of a resistor inserted in the emitter of the power transistor. The voltage obtained is applied on Pin 3 of the TEA2260/61.

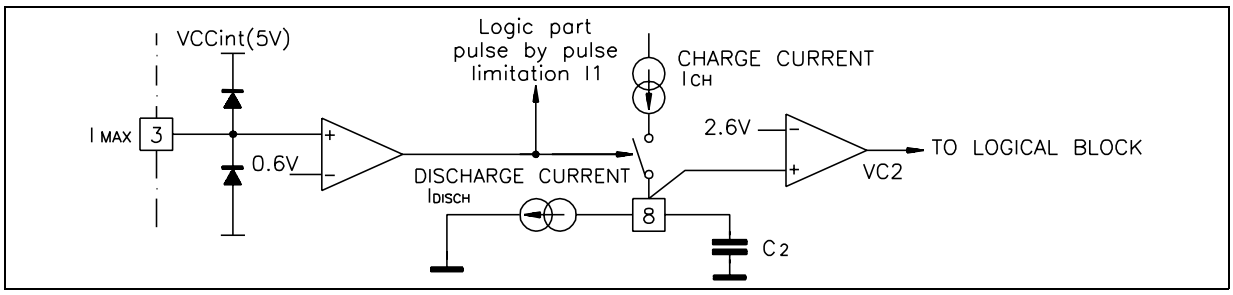
The current limitation device of the TEA2260/61 is a double threshold device. For the first threshold, there is no difference between the two devices, only for the second threshold.

Figure 21



II.8.1.1 - First threshold : VIM1 (typical value)

Figure 22 : Current Limitation Schematic Principle. First Threshold Part.



Two actions are carried out when the first threshold is reached

- The power transistor is switched-off (pulse by pulse limitation). A new conduction pulse is necessary to switch-on again.
- The C_2 capacitor, which is continuously discharged by Idisch current (10µA typically), is charged by the current
  Ich - I disch (45µA - 10µA = 35µA typically), until the next conduction pulse.

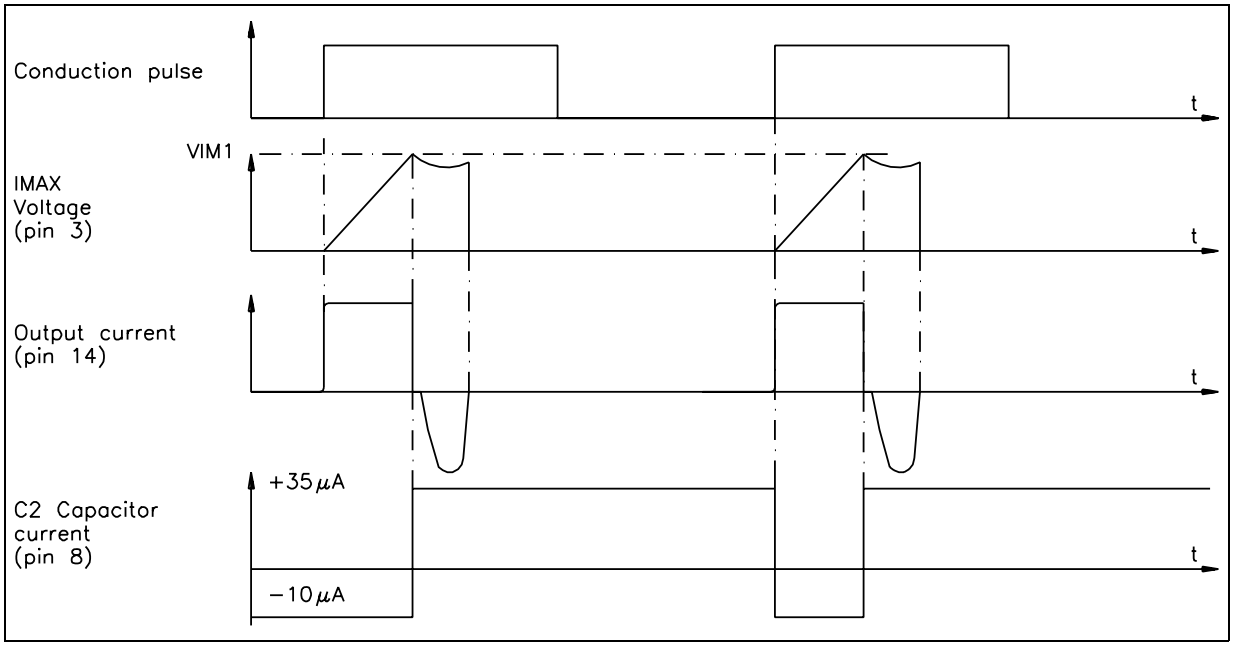
The capacitor C_2 is charged as long as an output overload is triggering the first current limitation threshold. When the voltage across C_2 reaches the threshold V_{C2} (typically 2.55V), output pulses (pin 14) are inhibited and the SMPS is stopped.

A restart may be obtained by decreasing Vcc under the $V_{CC(stop)}$ threshold to reset the IC.

If the output overload disappears before the voltage across C_2 reaches V_{C2}, the capacitor is discharged and the power supply is not turned off.

Due to this feature, a transient output overload is tolerated, depending on the value of C_2 (see III.2.5).

Figure 23 : Example of First Current Limitation Threshold Triggering



II.8.1.2 - Second current limitation threshold (VIM2) for TEA2260

In case of hard overload or short circuit, despite the pulse by pulse current limitation operation, the current in the power transistor continues to increase. If the second threshold VIM2 is reached, the power supply is immediately turned off and the internal counter is incremented. After 3 restarts, the power supply is definitively stopped.Restart is obtained by decreasing V_{CC} below $V_{CC(stop)}$, as in the case of stopping due to the repetitive overload protection triggering.

II.8.1.3 - Second current limitation threshold (VIM2) for TEA2261

For this device, if the second threshold is reached, the power supply is turned off, C_2 is charged and a new start-up is authorized only if $V_{C2} < 2.6V$.

II.8.2 - Logical Block

This block receives the safety signals coming from different blocks and inhibits the conduction signals when necessary.

II.8.2.1 - Logical block for TEA2260

TB is the conduction signal (primary or secondary)coming from the Is logical block.

TC is the conduction signal transmitted to the output stage.

I_1 is the output signal of the first current limitation threshold comparator. It is memorized by the flip-flop B1.

I_2 is the output signal of the second current limitation threshold comparator

V_{C2} is the output signal of the comparator checking the voltage across C2.

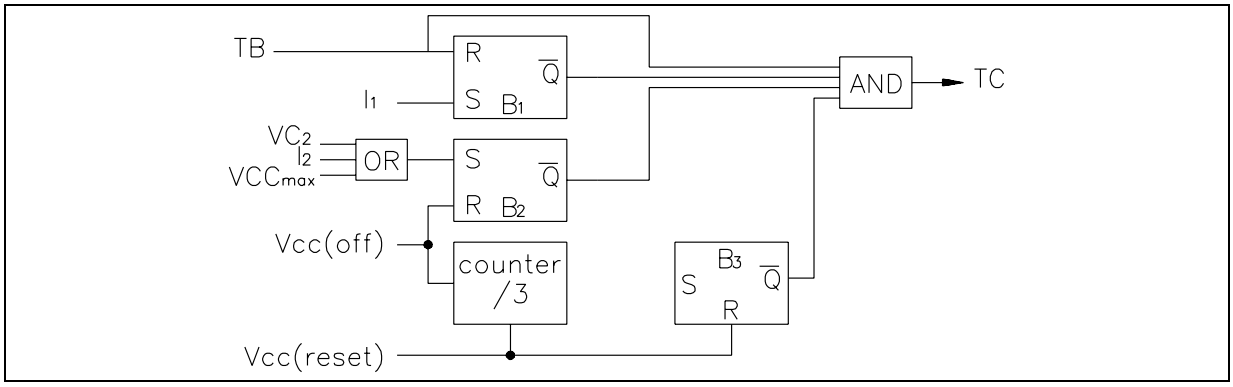
$V_{CC\ (Max.)}$ is the signal coming from V_{CC} checking comparator.

These three signals V_{C2}, I_2, $Vcc_{(max)}$ are memorized by B_2.

In case of B_2 flip-flop setting (I_2 or V_{C2} or $Vcc_{(max)}$ defect) the current consumption on V_{CC} increases. This function allows to decrease the Vcc voltage until $V_{CC(stop)}$). After this the current consumption on Vcc decreases to $I_{CC(start)}$ and a new start up is enabled.

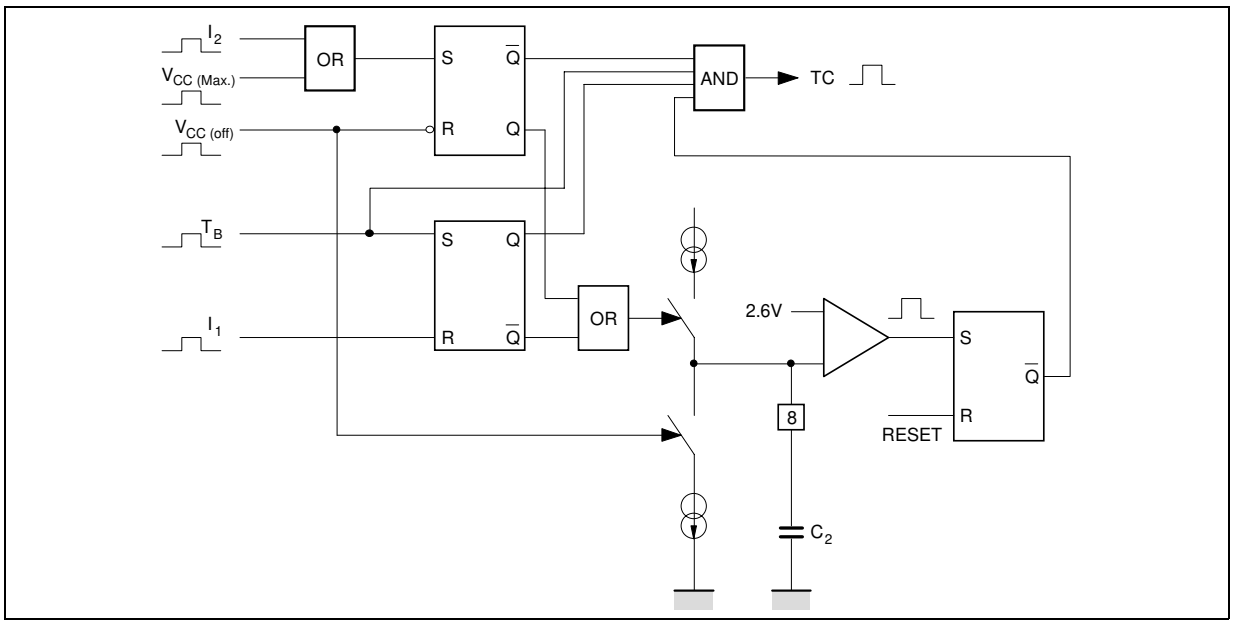
The $V_{CC(Off)}$ signal comes from the comparator checking V_{CC}. A counter counts the number of $V_{CC(off)}$ establishment. After four attempted starts of the power supply the output of the circuit is inhibited. To reset the circuit it is necessary to decrease V_{CC} below 5.5V typically. In practice this means that the power supply has to be disconnected from the mains.

Figure 24 : TEA2260 Simplified Logical Block Diagram



II.8.2.2 - Logical block for TEA2261

Figure 25



V_{CC}(off) is a signal coming from a comparator checking V_{CC}. When V_{CC} > V_{CC}(stop),V_{CE}(off) is high.

V_{CC}(max) is a signal coming from a comparator checking V_{CC}. When V_{CC} > V_{CC}(max),V_{CC}(max) is high.

I_1 is a signal coming from the first current limitation threshold comparator.
When I_{max} x R_{SHUNT} > VIM1, I_1 is high.

I_2 is a signal coming from the second current limitation threshold comparator.
When I_{max} x R_{SHUNT} > VIM2,I_2 is high.

TB is the conduction signal coming from the error ampliflier system.

TC is the output signal transmitted to the output stage.

II.9 - Output Stage

The output stage is made of a push-pull configuration : the upper transistor is used for power transistor conduction and the lower transistor for power transistor switch-off.

A capacitive coupling is recommanded in order to provide a sufficient negative base current through the power transistor .

Figure 26

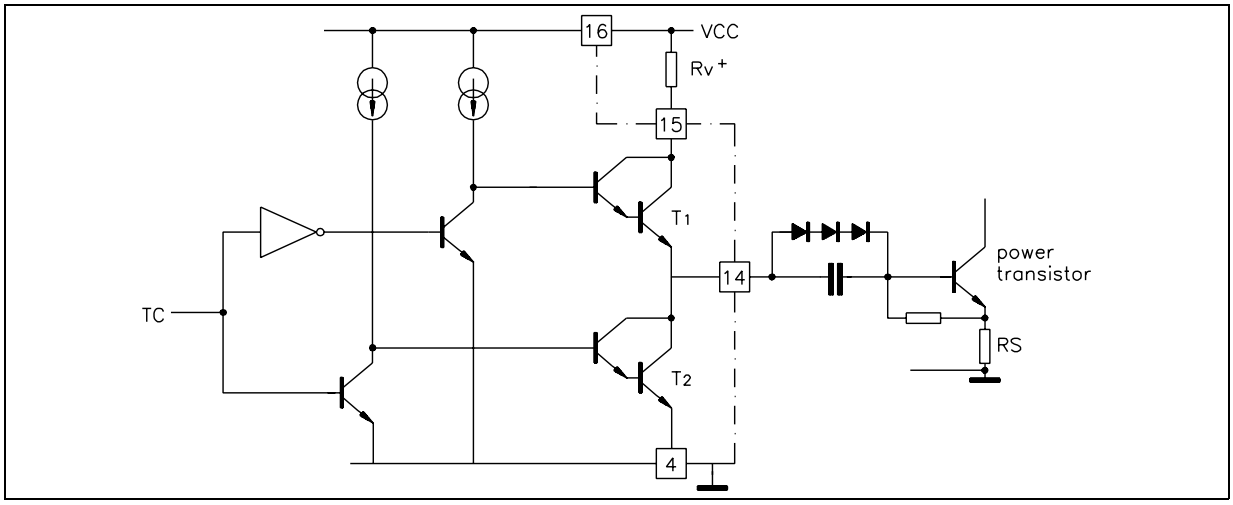
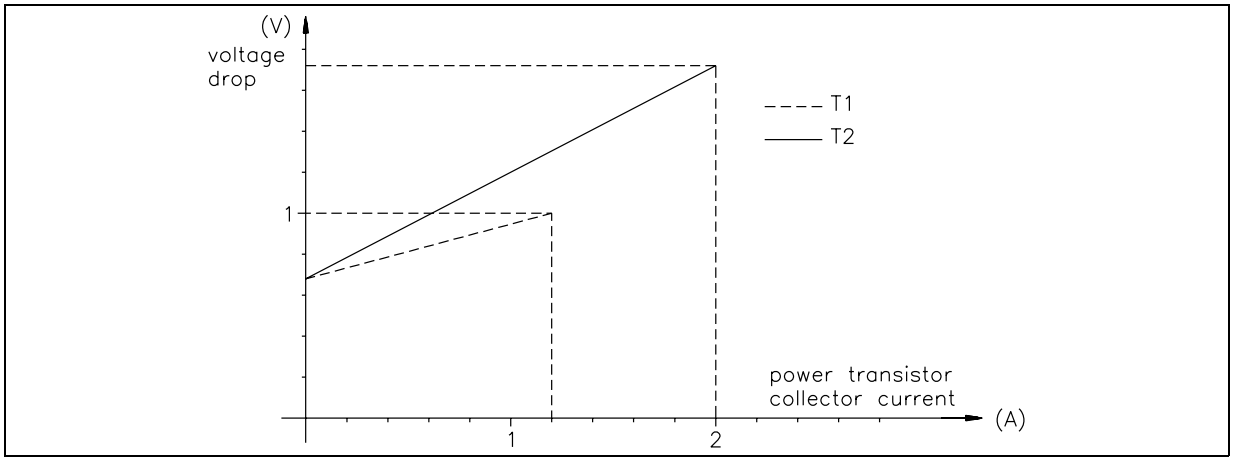


Figure 27 : Typical Voltage Drops of Output Transistor versus Current



Important remark : Due to the internal output stage structure, the output voltage (Pin 14) must never exceed 5V. This condition is respected when a bipolar transistor is driven.

Note that Power-MOS transistor drive is not possible with the TEA2260/61.

III - TV APPLICATION 120W - 220 VAC - 16kHZ SYNCHRONIZED ON HORIZONTAL DEFLECTION FREQUENCY

General structure and operational features of this power supply were outlined in section I.

The details covered below apply to a power supply application using the master circuit TEA5170.

(refer to TEA5170 data sheet and TEA5170 application note "AN088" for further details).

III.1 - Characteristics of Application

- Discontinuous mode Flyback SMPS
- Standby function using the burst mode of TEA2260/61
- Switching Frequency
  - Normal mode : 15.625 kHz (synchronized on horizontal deflection frequency)
  - Standby mode : about 16kHz
- Nominal mains voltage : 220 VAC

Mains voltage range : 170 VAC to 270 VAC

- Nominal output power : 120W
- Output power range in normal mode $14W < P_O < 120W$
- Output power range in standby mode $1W < P_O < 25W$
- Efficiency
- Normal mode : 85% (under nominal conditions)
- Stand by mode : 45%
- Regulation performance on high voltage output : 140 VDC
  - ± 0.3% versus mains variations of 170 VAC to 270 VAC (P_{OUT} : 120W)
  - ± 0.5% versus load variations of 14W to 120W (V_{in} = 220 VAC)
- Overload protection and complete shut down after a predetermined time interval.
- Short circuit protection.
- Open load protection by output overvoltage detection
- Complete power supply shut-down after 3 restarts resulting in the detection of a fault condition.
- Complete power supply shut-down when V_{C2} reaches 2.6V for TEA2261.

III.2 - Calculation of External Components

Also refer to TEA5170 application note "AN-088" for calculation methods applicable to other power supply components.

The external components to TEA2260/61 determine the following parameters :

- Operating Frequency in primary regulation
- Minimum conduction time in primary regulation
- Soft start duration
- overload duration
- Error amplifier gain and stand-by output voltage
- Base drive of the switching transistor
- Primary current limitation

Ideal values

- Free running Frequency in stand-by mode : 16kHz
- $Ton_{(min)}$ duration : 1µs
- Soft start duration : 30ms
- Maximum overload duration : 40ms
- Error amplifier Gain : 15
- Maximum primary current depends on the transformer specifications

III.2.1 - Transformer calculation

The following important features must be considered to calculate the specifications of the transformer :

- Maximum output power : 120W
- Minimum input voltage :
- 220 VAC - 20% → Vin(min) = 210 VDC with 40V ripple on the high voltage filtering capacitor
- Switching Frequency : 15.625kHz
- Maximum duty cycle : 0.45
- Output voltages :
  + 140V - 0.6A
  + 14V - 0.5A
  + 25V - 1A
  + 7.5V - 0.6A
  + 13V - 0.3A

Maximum primary current

$$I_{P(max)} = 2 \times \frac{P_{OUT}}{\eta \times V_{IN(min)} \times \frac{T_{ON(max)}}{T}}$$

η : efficiency of the power supply $0.80 < \eta < 0.85$

Primary inductance of the transformer

$$L_P = \frac{V_{IN(min)}}{I_{P(max)}} \times T_{ON(max)}$$

Transformer ratio

$$\frac{ns}{np} = \frac{(V_{OUT} + V_D) \times T_{DM}}{V_{IN(min)} \times T_{ON(max)}}$$

Reflected voltage

$$V_R = \frac{1}{\frac{T}{T_{ON(max)}} - 1} \times V_{IN(min)}$$

Overvoltage due to the leakage inductance

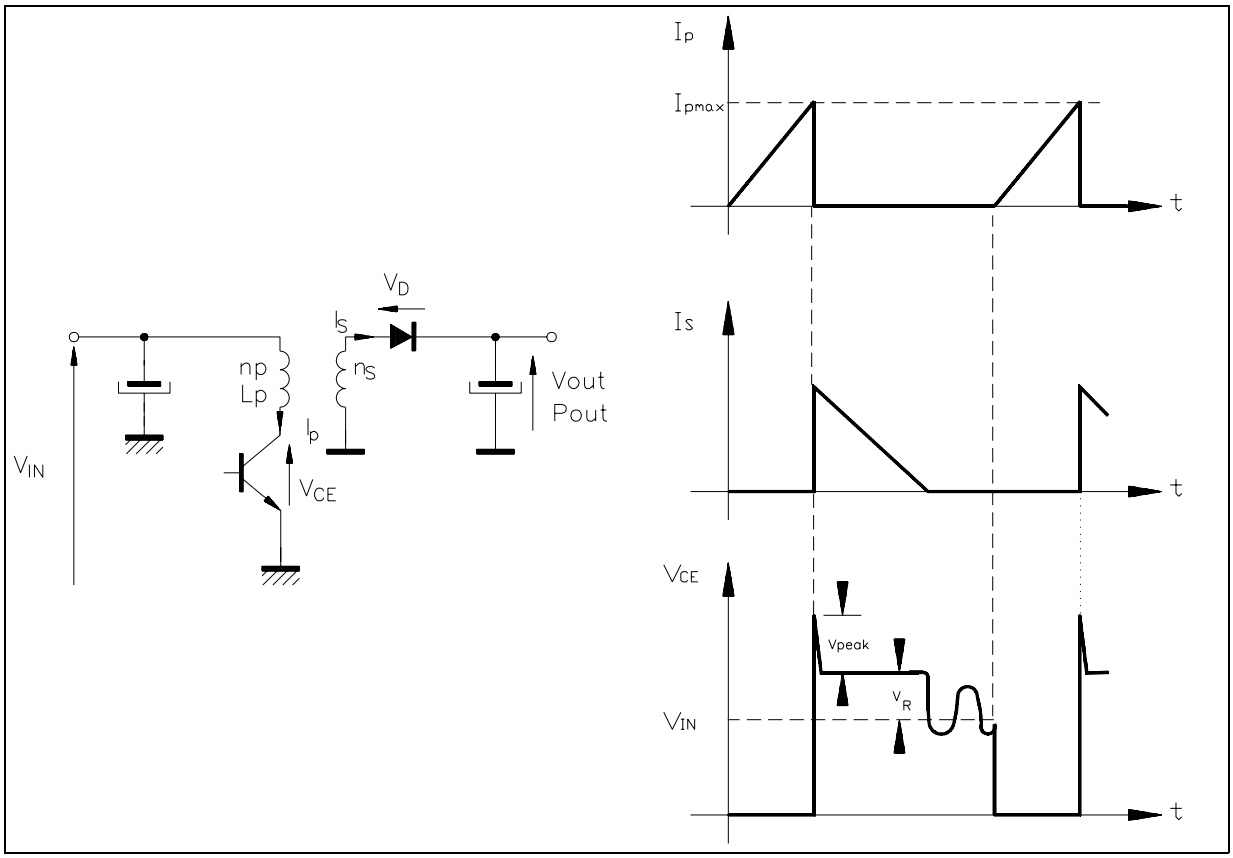
$$V_{PEAK} = \frac{I_{P(max)}}{2} \times \sqrt{\frac{L_f}{C}}$$

with : Lf = leakage inductance of the transformer

$$0.04 \times Lp < Lf < 0.10 \times Lp$$

C = capacitor of the snubber network (see III.2.2.2)

Figure 28



Numerical application

To determinate the specifications of the transformer, it is necessary to make a compromise between a maximum primary current and a maximum voltage on the transistor :

- To minimize the maximum primary current

with $0.4 < \frac{T_{ON(max)}}{T} < 0.5$

- To minimize the maximum voltage on the transistor during the demagnetization phase.

$0.3 < \frac{T_{ON(max)}}{T} < 0.4$

When the output power of the power supply is greater than 100W it is better to minimize the maximum primary current because the current gain $B_f = I_C / I_B$ of bipolar transistor is $1.5 < B_f < 6$

Choice : $\frac{T_{ON(max)}}{T} < 0.45$

$$I_{P(MAX)} = \frac{2 \times P_{OUT}}{\eta \times V_{IN(MIN)} \times \frac{T_{ON(MAX)}}{T}} = \frac{2 \times 120}{0.85 \times 210 \times 0.45} = 3A$$

$$L_P = \frac{V_{IN(MIN)}}{I_{P(MAX)}} \times T_{ON(MAX)} = \frac{210}{3} \times 0.45 \times 64\ 10^{-6} = 1.95mH$$

$$V_R = \frac{1}{\frac{T}{T_{ON(MAX)}} - 1} \times V_{IN(MIN)} = \frac{1}{\frac{1}{0.45} - 1} \times 210 = 172V$$

V_{PEAK} will be calculated with the snubber network determination (see II.2.2.2.1)

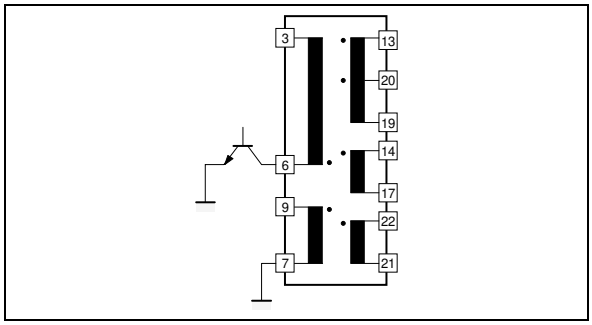
III.2.2 - Switching transistor and its base drive

III.2.2.1 - First current limitation

III.2.1.1 - Transformer specification

- Reference : OREGA - SMT5 - G4467-03
- Mechanical Data :
  - Ferrite : B50
  - 2 cores : 53 x 18 x 18 (mm) THOMSON-LCC
  - Airgap : 1.7 mm
- Electrical Data :

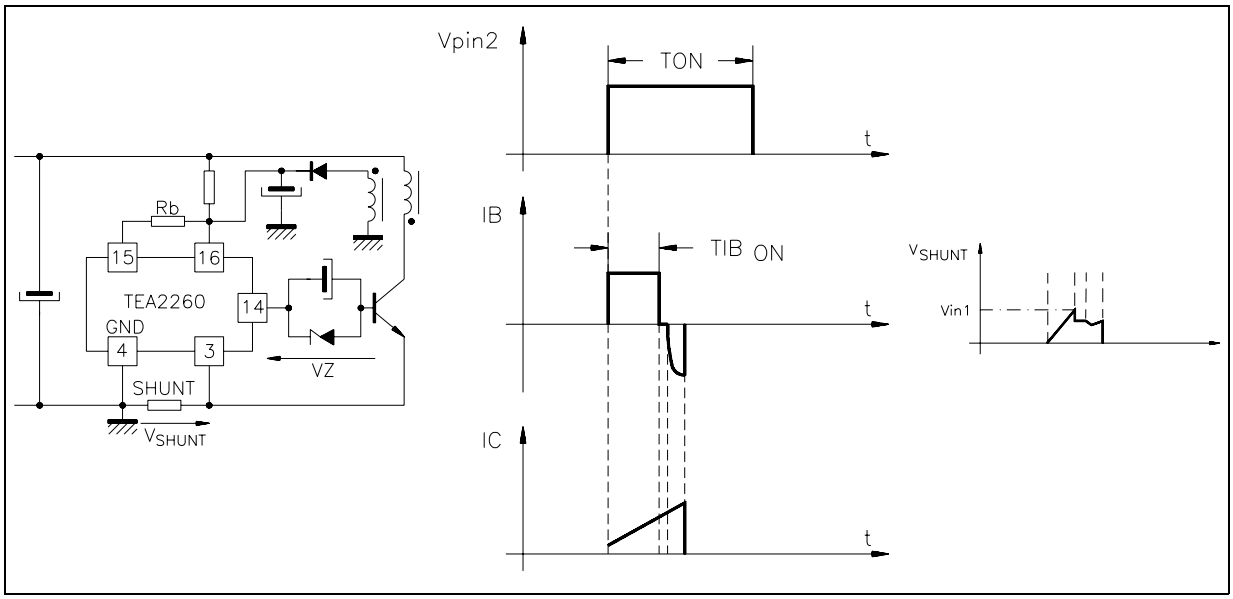
Figure 29



376-29.EPS

Winding	Pin	Inductance
n_P	3-6	1.95µH
n_{AUX}	7-9	8.1µH
n2	19-13	770µH
n3	19-20	8.2µH
n4	14-17	4.2µH
n5	22-21	31.7µH

Figure 30 : Current Limitation



376-30A.EPS / 376-30B.EPS / 376-30C.EPS

Note : in current limitation TIBon < T_{ON}

The current measurement is $I_E = I_B + I_C$

The maximum collector current calculated in III.2.1 is $I_{C(Max.)}$ = 3A (a switching transistor SGSF344 may be chosen)

The current gain is: $B_f = \frac{I_C}{I_{B+}} = 3.5$

The current limitation is :

$$I_{E(max)} = I_{P(max)} - (T_S \times \frac{V_{IN(min)}}{L_P}) + I_{B+}$$

with : T_S = storage time of the switching transistor (typ 3µs) and VIM1 = first threshold of current measurement (typ 0.6 v)

$$R_{SHUNT} = \frac{V_{IM1}}{I_{E(max)}}$$

Numerical application

$$I_{E(max)} = I_{P(max)} - (T_S \times \frac{V_{IN(min)}}{L_P}) + I_{B+}$$

$$I_{E(max)} = 3 - (3\ \ 10^{-6} \times \frac{210}{1.95\ \ 10^{-3}}) + 0.85 = 3.55A$$

$$R_{SHUNT} = \frac{V_{IM1}}{I_{E(max)}} = \frac{0.6}{3.255} = 0.169\Omega$$

III.2.2.2 - Snubber network

A R.D.C network is used to limit the overvoltage on the transistor during the switching off time.

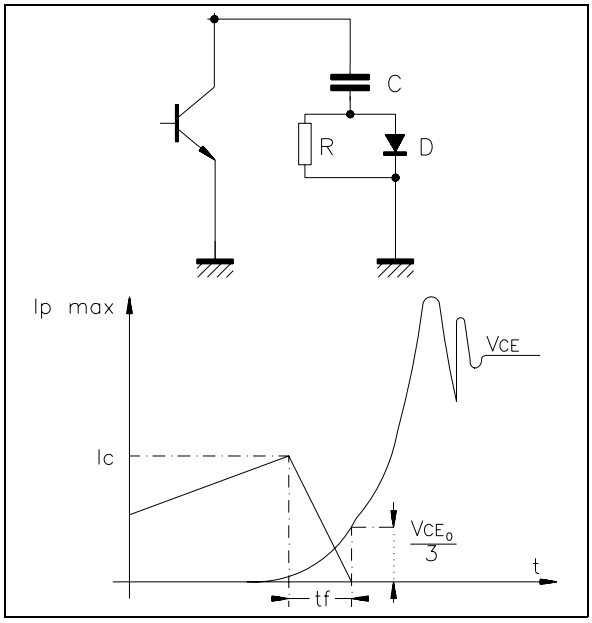
When the transistor is switched off, the capacitor is charged directly through the diode.

When the transistor is switched on, the capacitor is discharged through a resistor.

- $C = \frac{I_{P(max)} \times t_f}{2 \times \frac{VCE_O}{3}}$
- $3 \times R \times C = T_{on(min)}$ (to discharge the capacitor C by the correct amount)
- Maximum power dissipated in R :

$$P = \frac{1}{2} \times C \times (V_{IN(max)} + V_R)^2 \times F$$

Figure 31



376-31A.EPS / 376-31B.EPS

Numerical application (with SGSF 344 transistor) **with :**

$I_{P(Max.)}$ = 3A - $V_{IN(Max.)}$ = 370 VDC

t_f = 0.3µs - V_R = 172V

V_{CEO} = 600V - F = 16kHz

$T_{ON(Min.)}$ = 4µs

$$C = \frac{I_{P(max)} \times t_f}{2 \times \frac{VCE_O}{3}} = \frac{3 \times 0.3\ \ 10^{-6}}{2 \times \frac{600}{3}} = 2.25nF$$

$$R = \frac{T_{ON(min)}}{3 \times C} = \frac{4\ \ 10^{-6}}{3 \times 2.25\ \ 10^{-9}} = 560\Omega$$

$$P = \frac{1}{2} \times C \times V_{IN(max)} + V_R)^2 \times F$$

$$P = \frac{1}{2} \times 2.25 \cdot 10^9 \times (370 + 172)^2 \times 16 \cdot 10^3 = 5.29W$$

In the final application a value of 2.7nF is chosen to decrease the overvoltage on the transistor in short circuit condition.

III.2.2.2.1 - Overvoltage due to the leakage inductance (See. III.2.1)

The capacitor C of the snubber network influences the overvoltage due to the leakage inductance.

$$V_{peak} = \frac{I_{C(max)}}{2}\sqrt{\frac{L_f}{C}}$$

Numerical application

with : $L_f = 0.08 \times L_p = 0.08 \times 1.9\ 10^{-3} = 152\mu H$

$$V_{peak}\ \frac{3}{2} \times \sqrt{\frac{152\ 10^6}{2.25\ 10^9}} = 390V$$

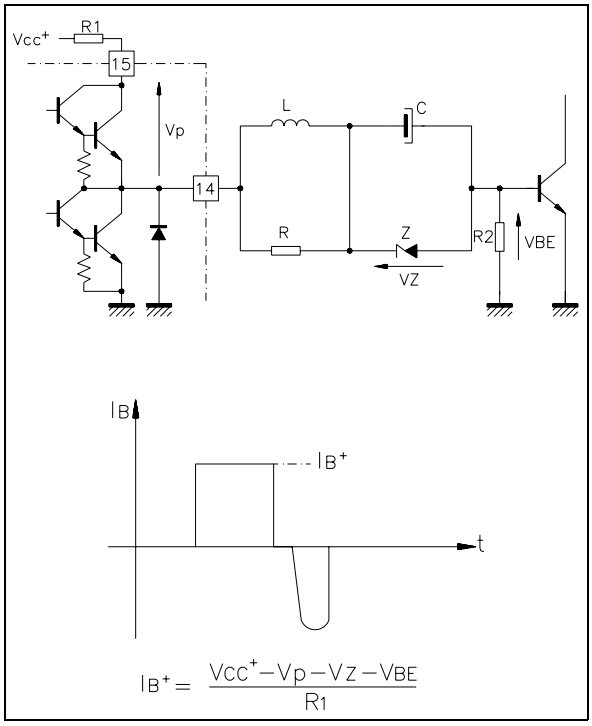
so $V_{CE(Max.)} = V_{IN(Max.)} + V_R + V_{peak} = V_{CE(Max.)} = 370 + 172 + 390 \cong 930V$

III.2.2.3 - Base drive

The output stage of the TEA2260/61 works in saturation mode and hence the internal power dissipation is very low.

$$R1 = \frac{V_{CC+} - V_P - V_Z - V_{BE}}{I_{B+}}$$

Figure 32

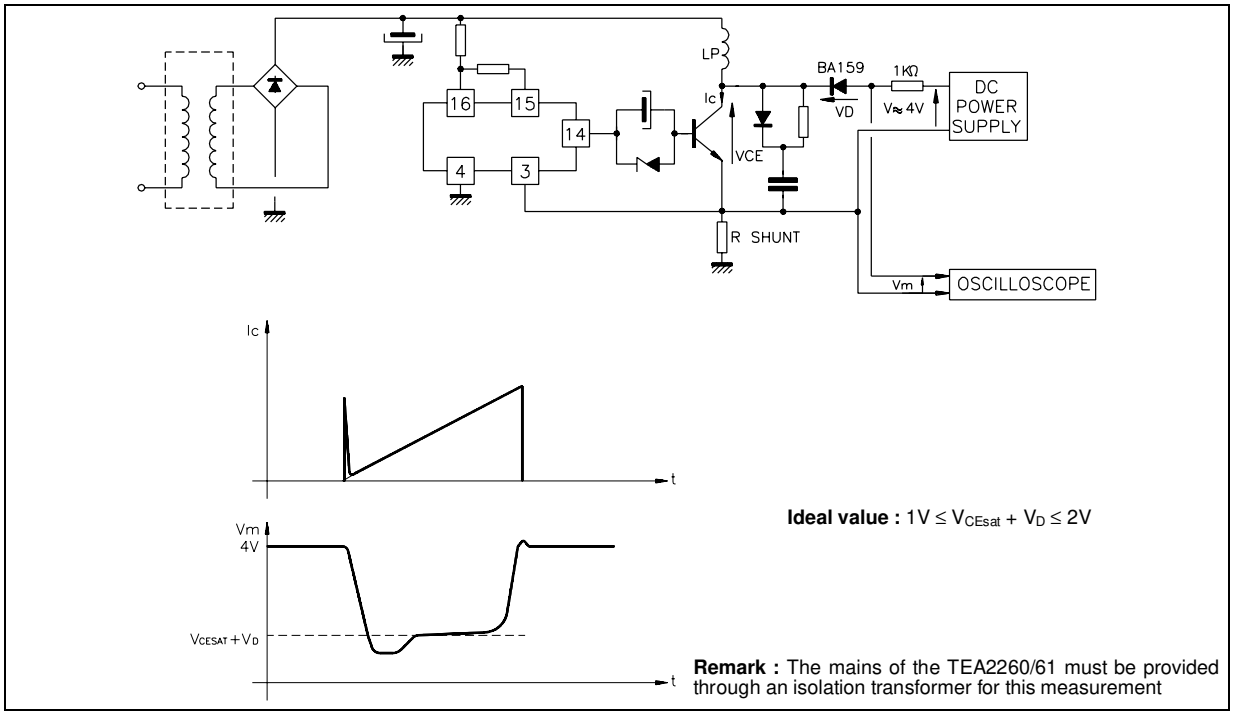


376-32A.EPS / 376-32B.EPS

Numerical application

$R1 = \frac{13 - 0.9 - 3 - 0.6}{0.85} \cong 10\Omega$ in this case the current gain, $BF = \frac{I_C}{I_B} = \frac{3}{0.85} = 3.5$ but it is recommanded to verify the VCE sat dynamic behaviour on the transistor as follows : see Figure 33

Figure 33



376-33A.EPS / 376-33B.EPS

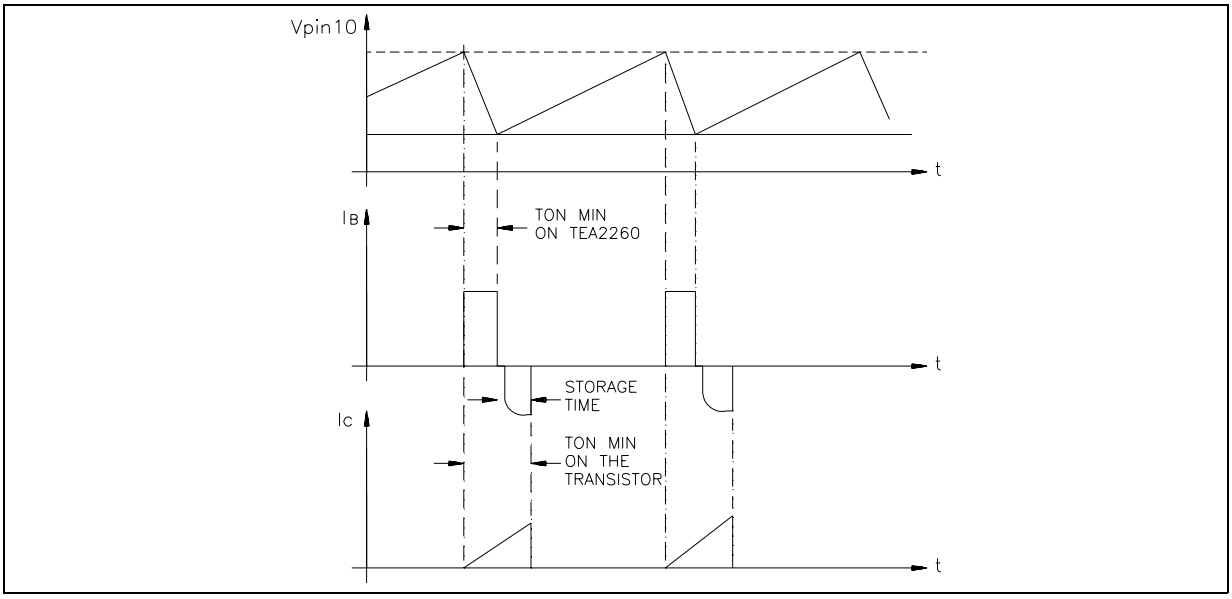
III.2.3 - Oscillator frequency

The free running frequency is given on II.2.

The typical value of minimum conduction time $T_{on(min)}$ on the output of the TEA2260/61 is given by: $T_{on(min)} = 1040 \times C_O$

Note : the minimum conduction time TON(min) on the transistor is longer due to the storage time.

Figure 34



Numerical application

F_O = 16kHz

C_O is chosen at 1nF

so T_{ON} min on the TEA2260/61 = 1µs

$$R_O = \frac{1}{F_O \times C_O \times 0.66} - 1.57\ 10^3$$

$$R_O = \frac{1}{16\ 10^3 \times 1\ 10^{-9} \times 0.66} - 1.57\ 10^3$$

R_O = 93 KΩ

R_O = 100kΩ is chosen.

Note : Fo is chosen relatively low to avoid magnetization of the transformer during the start-up phase.

III.2.4 - Regulation loop

In stand by mode the error amplifier of the TEA2260/61 carries out the regulation.

- The R.C. filter is necessary to avoid the peak voltage due to the leakage inductance. The time constant τ = RC is about 30µs < R.C. < 150µs as a function of the transformer technology.
- To achieve a stable behaviour of the regulation loop and to decrease the ripple on the output voltage in stand by mode the time constant should be approximately :

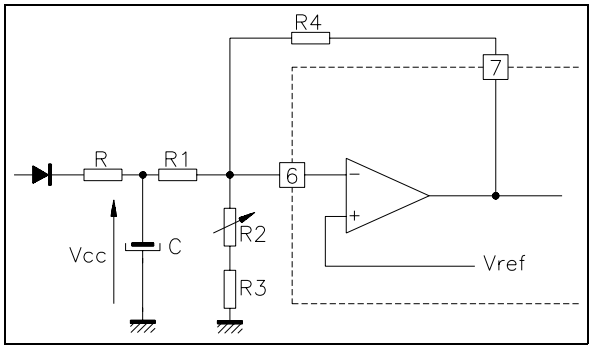
$$(R1 + R2 + R3) \times C \cong \frac{R_{OUT} \times C_{OUT}}{15}$$

with : C_{OUT} (filtering output capacitor) and R_{OUT} (load resistor on the output in stand by mode)

- To ensure a stable behaviour in stand-by mode the amplifier gain is choosen to :

$$G = \frac{R4}{R2 + R3} \cong 15$$

Figure 35



Calculation of R, R1, R2, R3, R4

a) The resistor R is given by

$$R = \frac{\tau}{C}$$

C choosen between 1µF < C < 10µF

τ = 80µs is chosen

C = 2.2µF is chosen

Numerical application

$$S_O R = \frac{\tau}{C} = \frac{80\ 10^{-6}}{2.2\ 10^{-6}} = 36\Omega$$

b) The resistors R1, R2, R3 are given by

$$R1 + R2 + R3 \cong \frac{C_{OUT} \times R_{OUT}}{15 \times C}$$

with :

V_{ref} : reference voltage of the error amplifier

$V_{ref} = 2.5V$

V_{cc}(stand by) : Vcc voltage in stand by mode.

V_{cc}(stand by) = 0.9 x V_{cc} (in normal mode)

Numerical application

with :

$V_{cc} = 13V$

$V_{ref} = 2.5V$

$R_{out} = 2k\ \Omega$ on output 135 V

$C_{out} = 100\mu F$ on output 135 V

$C = 2.2\mu F$

$$R1 + R2 + R3 \cong \frac{C_{OUT} \times R_{OUT}}{15 \times C} = \frac{100\ 10^{-6} \times 2\ 10^{3}}{15 \times 2.2\ 10^{-6}} = 6k\Omega$$

$$R2 + R3 = (R1 + R2 + R3) \times \frac{V_{REF}}{V_{CC}(\text{stand by})}$$

$$R2 + R3 = 6\ 10^{3} \times \frac{2.5}{0.9 \times 13} = 1.28k\Omega$$

values choosen :

R2 potentiometer resistor of 1kΩ

R3 fixed resistor 1kΩ

R1 = (R1+ R2 + R3) - (R2+ R3)

R1 = 6k - 1.28k = 4.7kΩ

c) The resistor R4 is given by $R4 \cong 15 \times (R2 + R3)$

Numerical application

$R4 \cong 15 \times (R2 + R3) \cong 15 \times (1.28\ 10^{3}) \cong 18k\Omega$

III.2.5 - Overload capacitor

When an overload is detected with the first threshold VIM1 the capacitor C2 (pin 8) is charged until the end of the period as shown in figure 33.

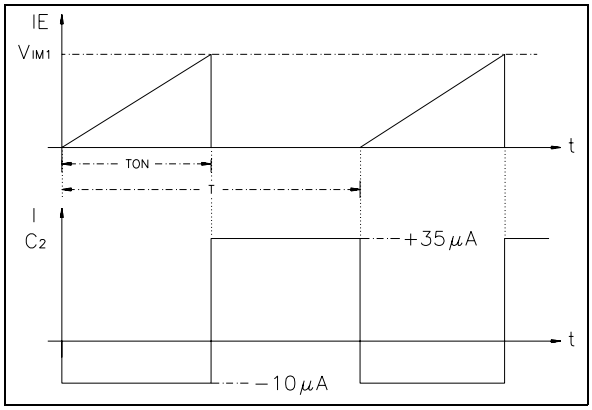
So the average load current is given by :

$$IC2 = \frac{T - T_{ON}}{T} \times I_{CH} - I_{DISH}$$

the threshold to cut off the TEA2260/61 power supply is 2.5V typically and hence the delay time before overload detection is given by :

$$Toverload = \frac{2.5 \times C2}{(\frac{T - T_{ON}}{T} \times I_{CH}) - I_{DISCH}}$$

Figure 36 : Load of Overload Capacitor



Numerical application

with : maximum overload time = 40 ms

the longer delay time is obtained when

$Ton = Ton_{(max)}$

$$C2 = ((\frac{T - Ton(max)}{T} \times I_{CH}) - I_{DISCH}) \times \frac{Toverload}{2.5}$$

$$C2 = (0.55 \times 45\ 10^{-6} - 10\ 10^{-6} \frac{40\ 10^{-3}}{2.5} \cong 220nF$$

Note : in practice, the overload capacitor value must be greater than the soft start capacitor (C2 ≥ C1) to ensure a correct start up phase of the power supply.

III.2.6 - Soft start capacitor

Refer to paragraph II.5 for the soft start function explanation.

The soft start duration is given by :

$$T_{SOFTSTART} = \frac{(2.7 - 1.5) \times C1}{9\ 10^{-6}}$$

$C1 = 7.5\ 10^{-6} \times T_{SOFTSTART}$

Numerical application

with : Tsoft start = 30 ms

$C1 = 7.5\ 10^{-6} \times 30\ 10^{-3} = 220$ nF

III.2.7 - Feed back voltage transformer

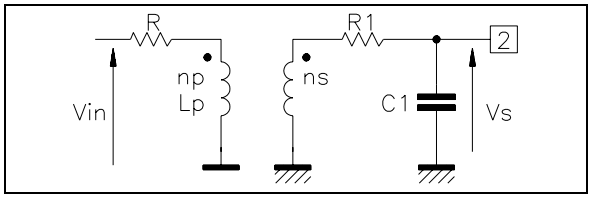
A feedback voltage transformer is used to send information from the secondary circuit (master circuit) to the primary circuit (slave circuit).

This transformer is needed to provide an electric insulation between primary and secondary side.

The feedback input of TEA2260/61 is fed with logic level (threshold 0.9V)

It is necessary to have the same waveform on the primary side as on the secondary side.

Figure 37



For this reason the time constant must be higher than the maximum conduction time in normal mode.
Hence the primary inductance Lp must be calculated as follows : $Lp > 3.R.T_{on(max)}$

Numerical application

with :

$T_{ON(max)} = 28\mu s$

$R = 270\Omega$

$L_p > 3 \times 270 \times 28\ 10^{-6} = 22mH$

a) When the TEA5170 is used $V_{IN} = 7V$

$$\frac{ns}{np} = \frac{V_{S(min)}}{V_{IN} \times (1 - \frac{T_{ON(max)}}{T})}$$

$$\frac{ns}{np} = \frac{1.5}{7 \times (1 - 0.45)} = 0.389$$

b) When the TEA 2028 is used $V_{IN} = 12V$

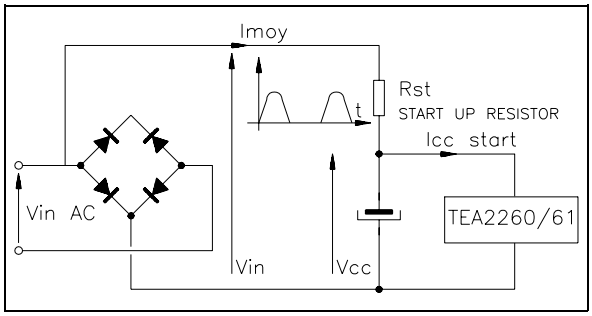
$$\frac{ns}{np} = \frac{1.5}{12 \times (1 - 0.45)} = 0.227$$

Note : The R1.C1 filter is used to damp oscillation on the secondary side of the feedback transformer. The time constant R1 x C1 ≅ 0.1µs.

III.2.8 - Start up resistor

After switching on the power supply the filtering capacitor on V_{CC} of TEA2260/61 is charged through a resistor connected to the mains input voltage. Do not connect this resistor to the high voltage filtering capacitor because there is enough energy in this capacitor to cause three attempted restarts and to cut off the TEA2260/61 on fault detection when the power supply is switched off. Hence it is recommended to connect the start-up resistor as follows :

Figure 38



Start up delay time

$$I_{MOY} = \frac{\sqrt{2} \times V_{IN\ AC(min)}}{\Pi \times R_{ST}}$$

$$\text{Start-up delay time} = Tst = \frac{V_{CC\ START}}{I_{MOY} - I_{CC\ START}} \times C$$

$$R_{ST} = \frac{\sqrt{2} \times V_{IN\ AC(min)}}{\Pi \times (C \times \frac{V_{CC\ START}}{T_{ST}}) + I_{CC\ START}}$$

Power dissipated in start up resistor

$$P = \frac{V_{IN\ AC(max)}2}{2\ .\ R_{ST}}$$

Numerical application

with :

start up delay time = 1s

$V_{IN(max)} = 370V$ DC ($V_{IN\ AC(max)} = 265V$)

$V_{IN\ AC(min)} = 175V$

$V_{ccstart} = 10.3V$

$I_{ccstart} = 0.7mA$

$C = 220\mu F$

$$R_{ST} = \frac{2 \times 175}{\Pi \times (220\ 10^{-6} \times 10.3 + 0.7\ 10^{-3})} = 26k\Omega$$

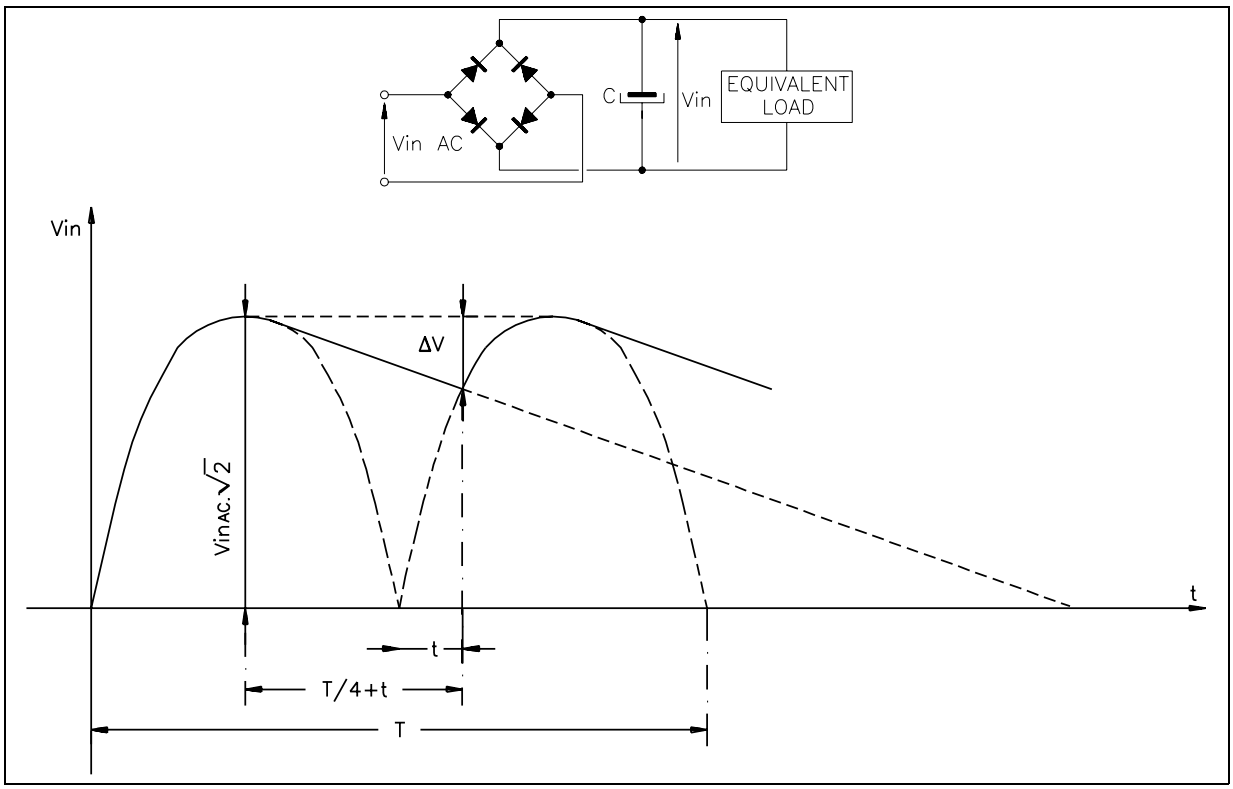
Value choosen = 22kΩ

Power dissipated

$$P = \frac{(265)^2}{2 \times 22\ 10^3} = 1.6W$$

III.2.9 - Determination of high voltage filtering capacitor

Figure 39



Hypothesis :

ΔV : ripple on the filtering voltage

$V_{IN.AC(min)}$: minimal value of A.C. input voltage

T : period of the mains voltage

P_{out} : output power of the power supply

η : efficiency of the power supply

$$C = \frac{T}{2\pi} \times \frac{\frac{\pi}{2} + \text{ArcSin}(1 - \frac{\Delta V}{V_{IN\,AC(min)} \times \sqrt{2}})}{\Delta V_{IN\,AC(min)} \times \sqrt{2}} \times \frac{P_{OUT}}{\eta}$$

Numerical application

$\Delta V = 40V$

$V_{IN\,AC(min)} = 170$ VAC

$T = 20ms$

$P_{OUT} = 120W$

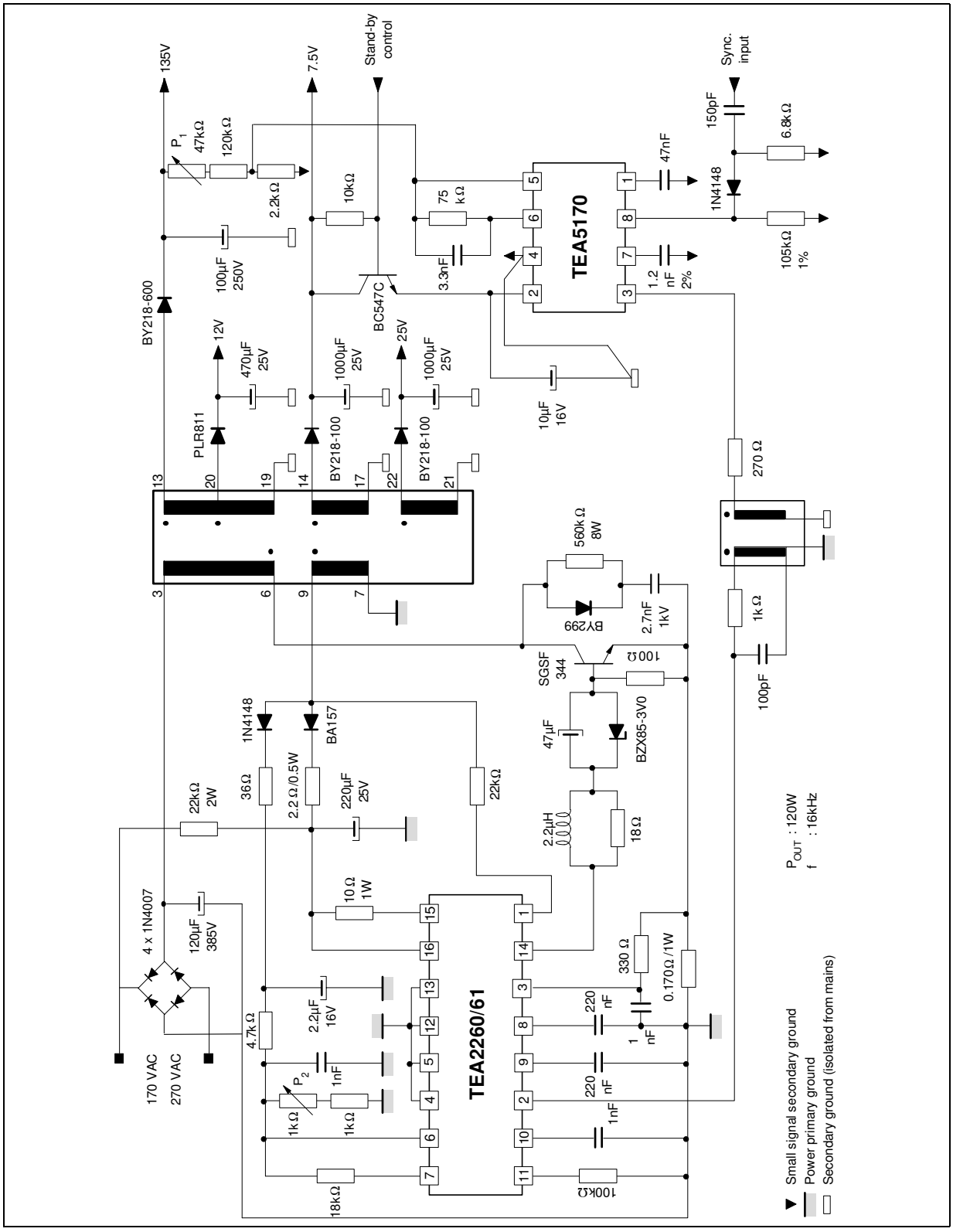
$\eta = 0.85$

$$C = \frac{20\ 10^{-3}}{2\pi} \times \frac{\frac{\pi}{2} + \text{ArcSin}(1 - \frac{40}{250})}{40 \times 250} \times \frac{120}{0.85} = 115\mu F$$

value choosen : C = 120µs

III.3 - Electrical Diagram

Figure 40



IV - TV APPLICATION 140W - 220 VAC - 32kHz SYNCHRONIZABLE

All details concerning the determination of external components are described in section III.

IV.1 - Application Characteristics

- Discontinuous mode flyback SMPS
- Stand-by function using the burst mode of TEA 2260.
- Switching frequency in burst mode : 16kHz
- Switching frequency in normal mode : 32kHz
- Nominal mains voltage : 220 VAC
- Mains voltage range : 170 VAC to 270 VAC
- Output power range in normal mode 25W < Po 140W
- Output power range in stand-by mode 2W < Po 45W
- Efficiency at full load > 80%
- Efficiency in stand-by mode (Po = 7W) > 50%
- Short circuit protection
- Long duration overload protection
- Complete shut down after 3 restarts with fault detection for TEA2260
- Complete shut down when V_{C2} reaches 2.6V for TEA2261

Load regulation **(VDC = 310V)**

Output 135V (+/- 0.18%) → (I_{135} : 0.01A to 0.8A; I_{25} = 1A)

Output 25V (+/- 2%) → (I_{135} : O.8A; I_{25} = 0.5A to 1A)

Line regulation **($I1_{35}$: 0.8A; I_{25} : 1A)**

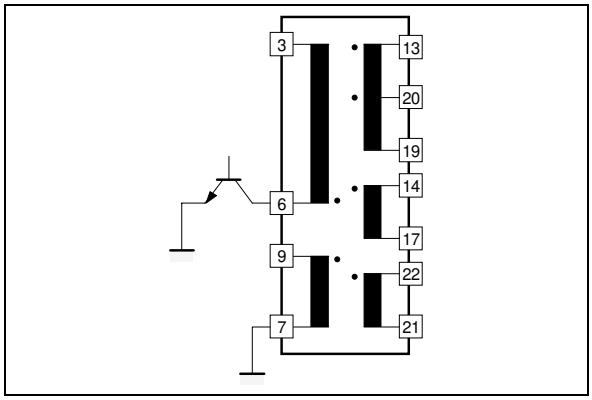
Output 135V (+/- 0.13%)→ (210V < V_{DC} < 370V)

Output 25V (+/- 0.17%)

IV.2 - Transformer Specification

- Reference : OREGA.SMT5. G4576-03
- Electrical Data :

Figure 41

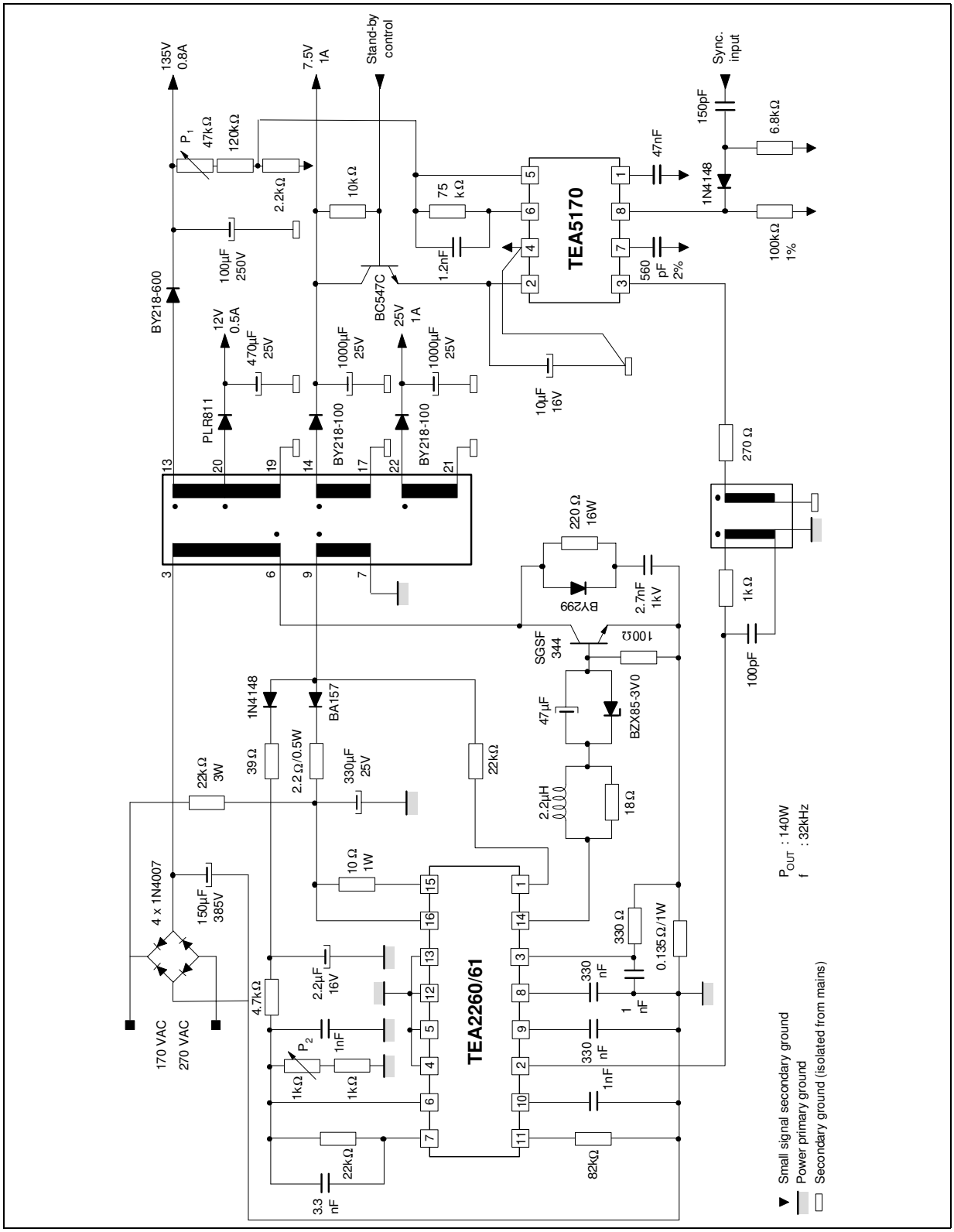


376-41.EPS

Winding	Pin	Inductance
n_P	3-6	790µH
n_{AUX}	7-9	5.4µH
n2	19-13	338µH
n3	19-20	4.8µH
n4	14-17	3.4µH
n5	22-21	13µH

IV.3 - Electrical Diagram

Figure 42



V - TV APPLICATION 110W -220 VAC - 40kHz REGULATED WITH OPTOCOUPLER

This application works in asynchronous mode. The regulation characteristics are very attractive (output power variation range from 1W to 110W due to automatic burst mode (see II.6). In this configuration higher is the regulation loop gain, lower is the output voltage ripple in burst mode (e.g. ouput voltage ripple 0.8% with a loop gain of 15).

V.1 - Frequency Soft Start

The nominal switching frequency is 40kHz but during the start-up phase the switching frequency is shifted to 10kHz in order to avoid the magnetization of the transformer.

Otherwise the second current limitation will be reached at high input voltage and hence the power supply will not start.

V.2 - Application Characteristics

- Discontinous mode Flyback SMPS
- Switching frequency : 40kHz
- Nominal mains voltage : 220 VAC
- Mains voltage range : 170 VAC to 220 VAC
- Output power in normal mode : 30W < Po < 110W
- Output power in burst mode : 1W < Po < 30W.The transient phase between normal mode and burst mode is determinated automatically as a function of the output power. Hence the regulation of the output voltage is effective for an output power variation of 1W < Po < 110W
- Efficiency as full load > 80%
- Efficiency in burst mode (Po = 8W) > 50%
- Short circuit protection
- Open load protection
- Long duration overload protection
- Complete shutdown after 3 restarts with fault detection for TEA2260
- Complete shut down when V_{C2} reaches 2.6V for TEA2261

Load regulation *(VDC = 310V)*

Output 135V (+/- 0.15%) → (I_{135} : 0.05A to 0.6A; I_{25} = 1A)
Output 25V (+/- 2.5%) →(I_{135} = 0.6A; I_{25} : 0.25 to 1A)

Line regulation *(I_{135} : 0.6A; I_{25} : 1A)*

Output 135V (+/- 0.30%) → (210V < VDC <, 370V)
Output 25V (+/- 0.30%)

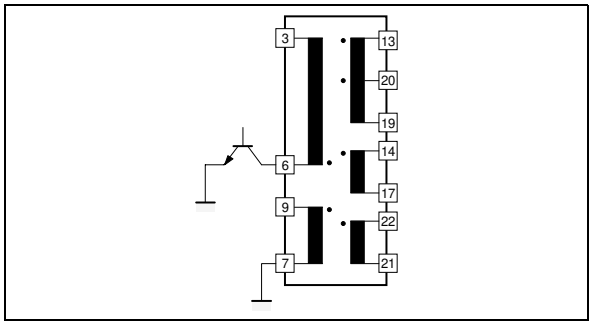
Influence of the audio output on the video output

Output 135V (+/- 0.1%) →(I_{135} = 0.6A; I_{25} : 0 →1A)
Output 135V (+/- 0.05%) →(I_{135} = 0.3A; I_{25} : 0 →1A

V.3 - Transformer Specification

- Reference : OREGA.SMT5. G4576-02
- Mechanical Data :
  - Ferrite : B50
  - 2 cores : 53 x 18 x 18(mm) THOMSON LCC
- Electrical Data :

Figure 43

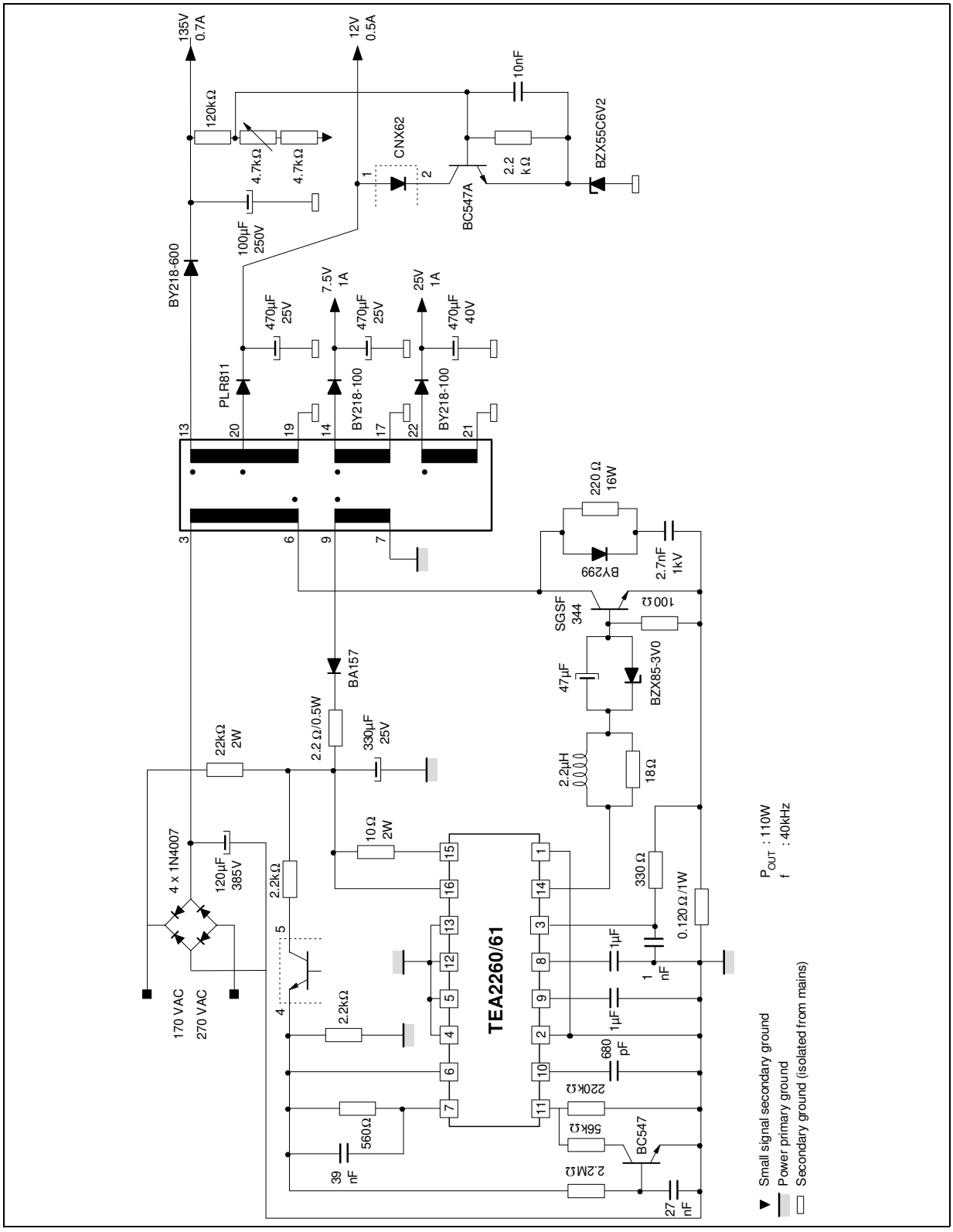


376-43.EPS

Winding	Pin	Inductance
n_P	3-6	790µH
n_{AUX}	7-9	5.4µH
n2	19-13	338µH
n3	19-20	4.8µH
n4	14-17	3.4µH
n5	22-21	13µH

V.4 - Electrical Diagram

Figure 44



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