MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

*Advance Information*

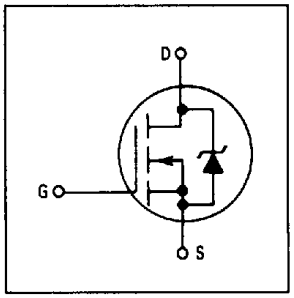
# TMOS IV
# N-Channel Enhancement-Mode
## Power Field Effect Transistor

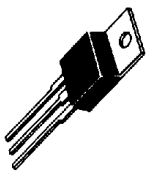
**MTP3055E**
Motorola Preferred Device

**TMOS POWER FET**
**12 AMPERES**
**$R_{DS(on)}$ = 0.15 OHM**
**60 VOLTS**


This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits.
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode.
- Diode is Characterized for Use in Bridge Circuits.



**CASE 221A-06**
**TO-220AB**

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**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | MTP3055E | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain-Gate Voltage ($R_{GS}$ = 1 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate-Source Voltage — Continuous<br>— Non-repetitive ($t_p \leq 50\ \mu s$) | $V_{GS}$<br>$V_{GSM}$ | ±20<br>±40 | Vdc<br>Vpk |
| Drain Current — Continuous<br>— Pulsed | $I_D$<br>$I_{DM}$ | 12<br>26 | Adc |
| Total Power Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 40<br>0.32 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | −65 to 150 | °C |

**THERMAL CHARACTERISTICS**

| | | | |
|---|---|---|---|
| Thermal Resistance — Junction to Case<br>— Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 3.12<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds | $T_L$ | 260 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | |
| Drain-Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 0.25 mA) | $V_{(BR)DSS}$ | 60 | — | Vdc |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = Rated $V_{DSS}$, $V_{GS}$ = 0)<br>($V_{DS}$ = Rated $V_{DSS}$, $V_{GS}$ = 0, $T_J$ = 125°C) | $I_{DSS}$ | —<br>— | 10<br>80 | μA |

(continued)

This document contains information on a new product. Specifications and information herein are subject to change without notice.

**Preferred** device is a Motorola recommended choice for future use and best overall value.

**ELECTRICAL CHARACTERISTICS — continued** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **OFF CHARACTERISTICS (continued)** | | | | |
| Gate-Body Leakage Current, Forward ($V_{GSF}$ = 20 Vdc, $V_{DS}$ = 0) | $I_{GSSF}$ | — | 100 | nAdc |
| Gate-Body Leakage Current, Reverse ($V_{GSR}$ = 20 Vdc, $V_{DS}$ = 0) | $I_{GSSR}$ | — | 100 | nAdc |
| **ON CHARACTERISTICS*** | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 1 mA)<br>$T_J$ = 100°C | $V_{GS(th)}$ | <br>2<br>1.5 | <br>4.5<br>4 | Vdc |
| Static Drain-Source On-Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 6 Adc) | $R_{DS(on)}$ | — | 0.15 | Ohm |
| Drain-Source On-Voltage ($V_{GS}$ = 10 V)<br>($I_D$ = 12 Adc)<br>($I_D$ = 6 Adc, $T_J$ = 100°C) | $V_{DS(on)}$ | <br>—<br>— | <br>2<br>1.5 | Vdc |
| Forward Transconductance ($V_{DS}$ = 15 V, $I_D$ = 6 A) | $g_{FS}$ | 4 | — | mhos |
| **DRAIN-TO-SOURCE AVALANCHE STRESS CAPABILITY** | | | | |
| Unclamped Inductive Switching Energy See Figures 15 and 16<br>($I_D$ = 26 A, $V_{DD}$ = 6 V, $T_C$ = 25°C, Single Pulse, Non-repetitive)<br>($I_D$ = 12 A, $V_{DD}$ = 6 V, $T_C$ = 25°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%)<br>($I_D$ = 4.8 A, $V_{DD}$ = 6 V, $T_C$ = 100°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%) | $W_{DSR}$ | <br>—<br>—<br>— | <br>18<br>35<br>16 | mJ |
| **DYNAMIC CHARACTERISTICS** | | | | |
| Input Capacitance | ($V_{DS}$ = 25 V, $V_{GS}$ = 0, f = 1 MHz) See Figure 11 | $C_{iss}$ | — | 500 | pF |
| Output Capacitance | | $C_{oss}$ | — | 300 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | — | 100 | |
| **SWITCHING CHARACTERISTICS*** ($T_J$ = 100°C) | | | | | |
| Turn-On Delay Time | ($V_{DD}$ = 25 V, $I_D$ = 0.5 Rated $I_D$, $R_{gen}$ = 50 ohms) See Figure 18 | $t_{d(on)}$ | — | 20 | ns |
| Rise Time | | $t_r$ | — | 60 | |
| Turn-Off Delay Time | | $t_{d(off)}$ | — | 65 | |
| Fall Time | | $t_f$ | — | 65 | |
| Total Gate Charge | ($V_{DS}$ = 0.8 Rated $V_{DSS}$, $I_D$ = Rated $I_D$, $V_{GS}$ = 10 V) See Figure 14 | $Q_g$ | 12 (Typ) | 17 | nC |
| Gate-Source Charge | | $Q_{gs}$ | 6.5 (Typ) | — | |
| Gate-Drain Charge | | $Q_{gd}$ | 5.5 (Typ) | — | |
| **SOURCE DRAIN DIODE CHARACTERISTICS*** | | | | | |
| Forward On-Voltage | ($I_{FM}$ = 0.5 Rated $I_D$, $dI_S/dt$ = 100 A/μs, $V_{GS}$ = 0) | $V_{SD}$ | 1.7 (Typ) | 2 | Vdc |
| Forward Turn-On Time | | $t_{on}$ | Limited by stray inductance | | |
| Reverse Recovery Time | | $t_{rr}$ | 50 (Typ) | 90 | ns |
| **INTERNAL PACKAGE INDUCTANCE (TO-220)** | | | | | |
| Internal Drain Inductance<br>(Measured from the contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | $L_d$ | <br>3.5 (Typ)<br>4.5 (Typ) | <br>—<br>— | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad.) | $L_s$ | 7.5 (Typ) | — | |

*Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.

## TYPICAL ELECTRICAL CHARACTERISTICS

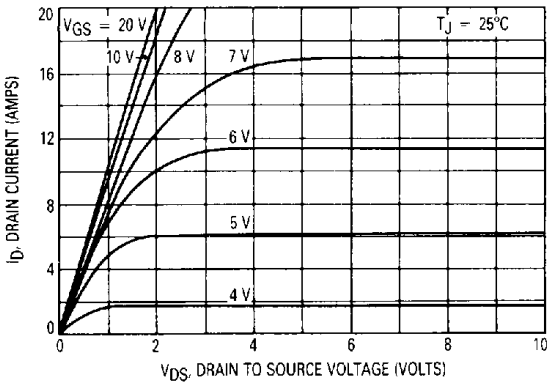



Figure 1. On-Region Characteristics

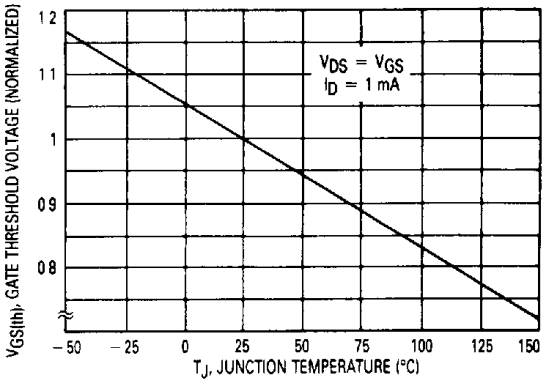



Figure 2. Gate-Threshold Voltage Variation With Temperature

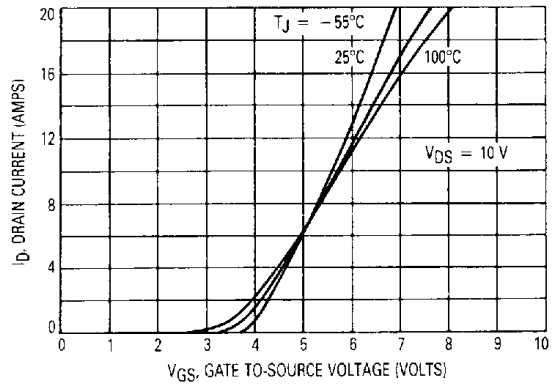



Figure 3. Transfer Characteristics

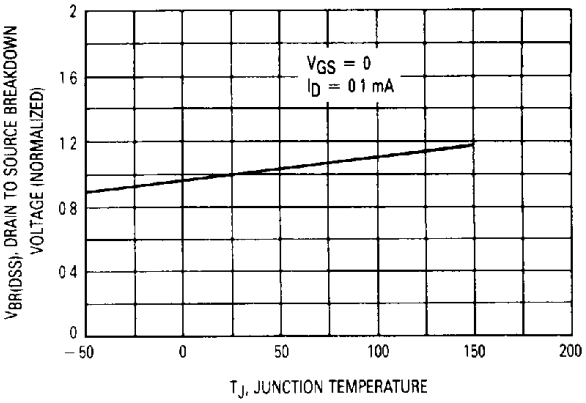



Figure 4. Breakdown Voltage Variation With Temperature

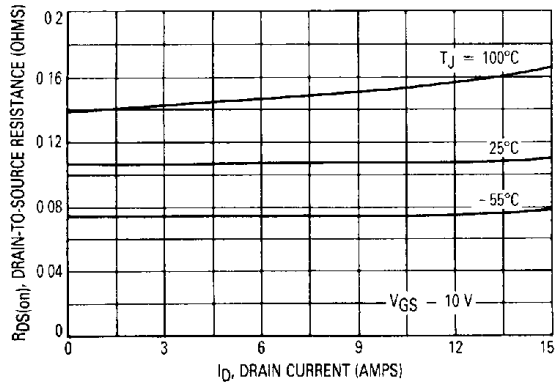



Figure 5. On-Resistance versus Drain Current

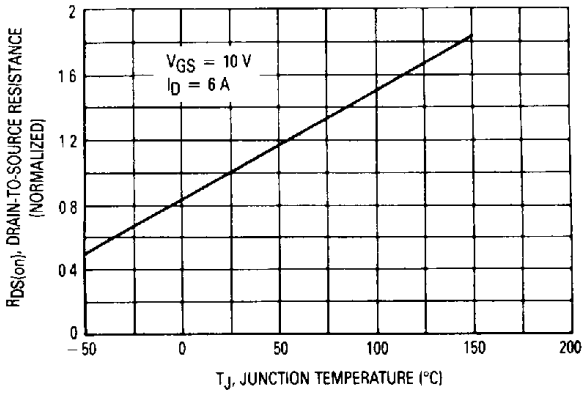



Figure 6. On-Resistance Variation With Temperature

## SAFE OPERATING AREA INFORMATION

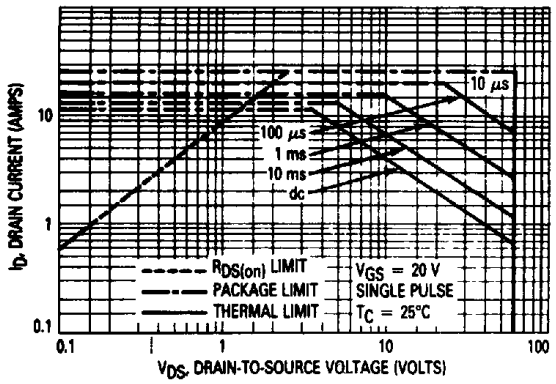



**Figure 7. Maximum Rated Forward Biased Safe Operating Area**

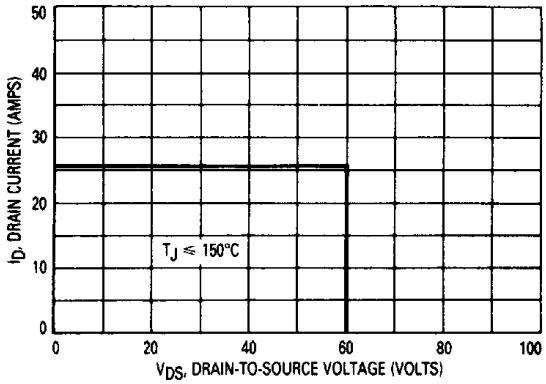



**Figure 8. Maximum Rated Switching Safe Operating Area**

### FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

### SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{DM}$ and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

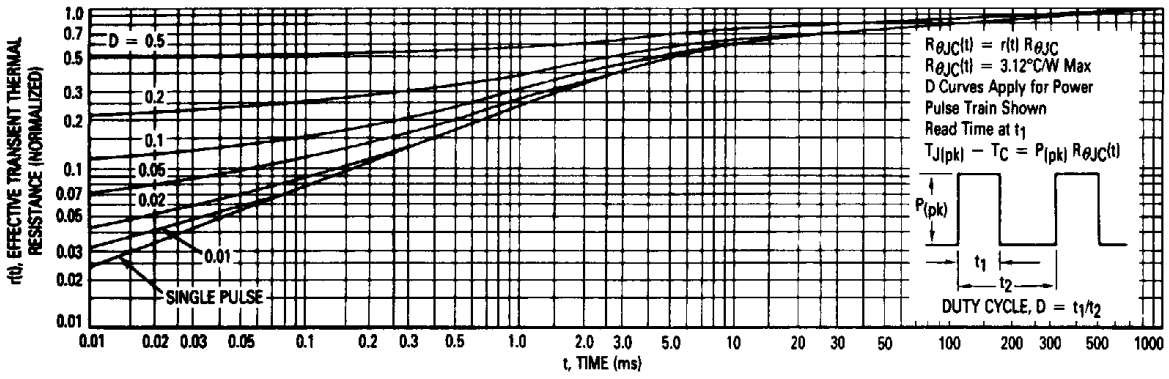



**Figure 9. Thermal Response**

## COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of $I_{FM}$ and peak $V_R$ for a given commutation speed. It is applicable when waveforms similar to those of Figure 10 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval $t_{frr}$ is the speed of the commutation cycle. Device stresses increase with commutation speed, so $t_{frr}$ is specified with a minimum value. Faster commutation speeds require an appropriate derating of $I_{FM}$, peak $V_R$ or both. Ultimately, $t_{frr}$ is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during $t_{rr}$ as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; $I_{FM}$ is the maximum forward source-drain diode current just prior to the onset of commutation.

$V_R$ is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as $I_S$ decays from $I_{RM}$ to zero

$R_{GS}$ should be minimized during commutation. $T_J$ has only a second order effect on CSOA.

Stray inductances, $L_i$ in Motorola's test circuit are assumed to be practical minimums.

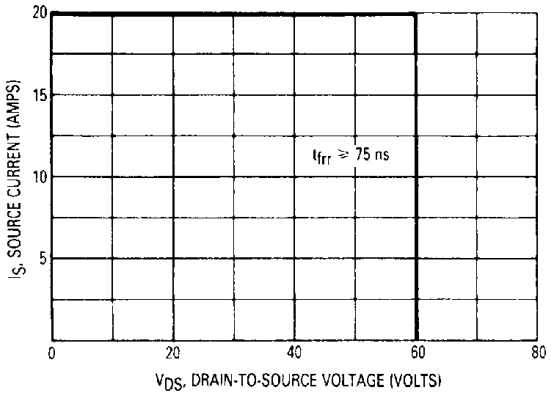



**Figure 11. Commutating Safe Operating Area (CSOA)**

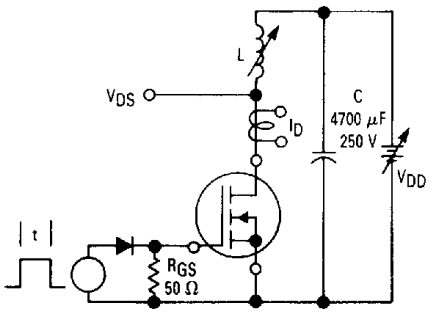



**Figure 13. Unclamped Inductive Switching Test Circuit**

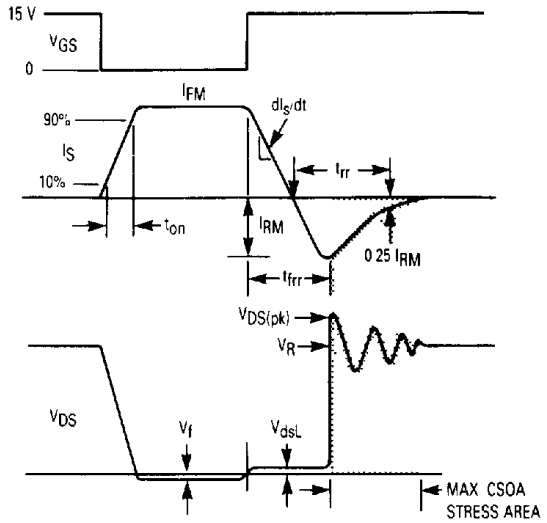



**Figure 10. Commutating Waveforms**

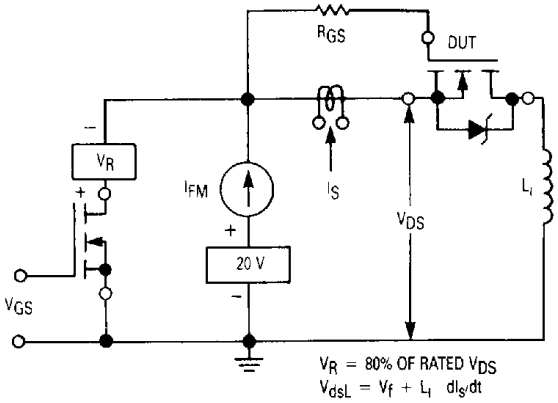



**Figure 12. Commutating Safe Operating Area Test Circuit**

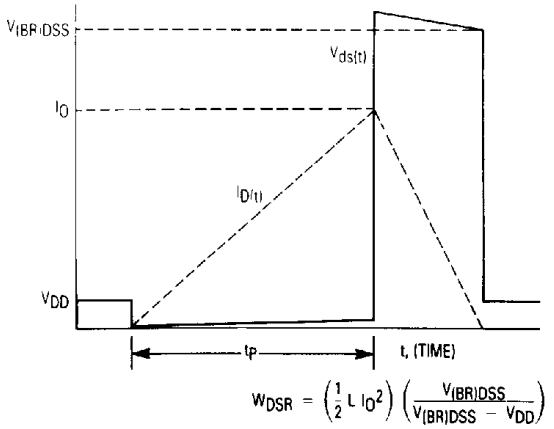



**Figure 14. Unclamped Inductive Switching Waveforms**

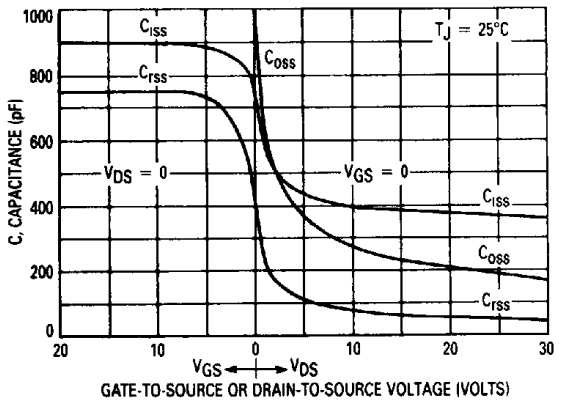



**Figure 15. Capacitance Variation**

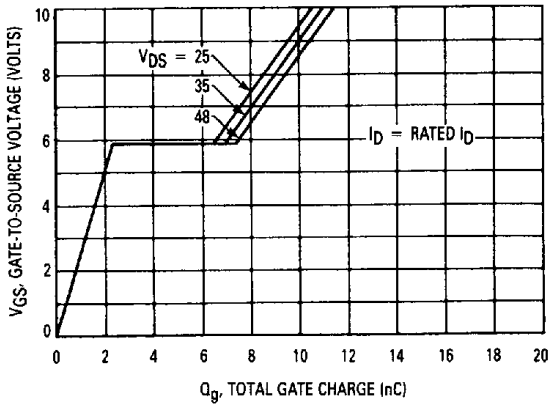
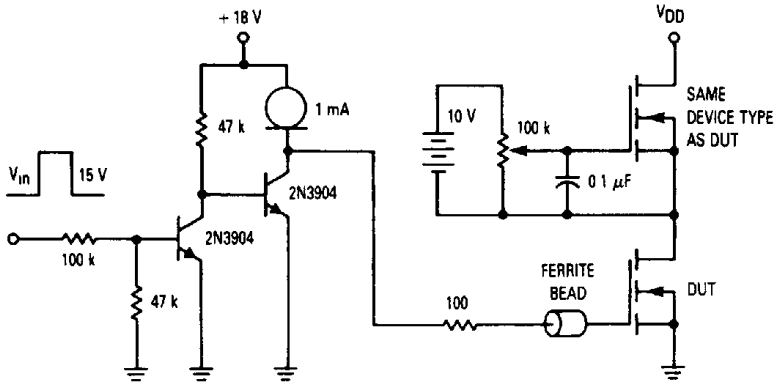



**Figure 16. Gate Charge versus Gate-to-Source Voltage**




$V_{in}$ = 15 $V_{pk}$, PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

**Figure 17. Gate Charge Test Circuit**