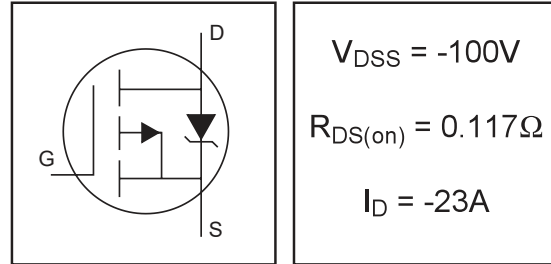


# IRFP9140NPbF

HEXFET<sup>®</sup> Power MOSFET

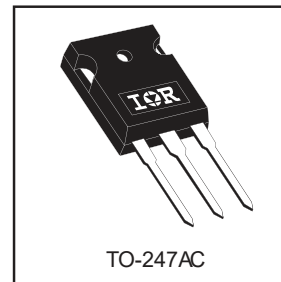
- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- P-Channel
- Fast Switching
- Fully Avalanche Rated
- Lead-Free



## Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.



## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-23	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-16	
$I_{DM}$	Pulsed Drain Current ①⑤	-76	
$P_D @ T_C = 25^\circ C$	Power Dissipation	140	W
	Linear Derating Factor	0.91	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy②⑤	430	mJ
$I_{AR}$	Avalanche Current①	-11	A
$E_{AR}$	Repetitive Avalanche Energy①	14	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑥	-5.0	V/ns
$T_J$	Operating Junction and Storage Temperature Range	-55 to + 175	°C
$T_{STG}$			
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

## Thermal Resistance

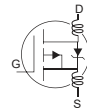
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.1	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

# IRFP9140NPbF

International  
 Rectifier

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-100	—	—	V	$V_{GS} = 0\text{V}$ , $I_D = -250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.11	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}$ , $I_D = -1\text{mA}$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.117	$\Omega$	$V_{GS} = -10\text{V}$ , $I_D = -13\text{A}$ ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	$V_{DS} = V_{GS}$ , $I_D = -250\mu\text{A}$
$g_{fs}$	Forward Transconductance	5.3	—	—	S	$V_{DS} = -50\text{V}$ , $I_D = 11\text{A}$ ⑤
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	-25	$\mu\text{A}$	$V_{DS} = -100\text{V}$ , $V_{GS} = 0\text{V}$ $V_{DS} = -80\text{V}$ , $V_{GS} = 0\text{V}$ , $T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -20\text{V}$
$Q_g$	Total Gate Charge	—	—	97	nC	$I_D = -11\text{A}$ $V_{DS} = -80\text{V}$ $V_{GS} = -10\text{V}$ , See Fig. 6 and 13 ④ ⑤
$Q_{gs}$	Gate-to-Source Charge	—	—	15	nC	
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	51	nC	
$t_{d(on)}$	Turn-On Delay Time	—	15	—	ns	$V_{DD} = -50\text{V}$ $I_D = -11\text{A}$ $R_G = 5.1\Omega$ $R_D = 4.2\Omega$ , See Fig. 10 ④ ⑤
$t_r$	Rise Time	—	67	—		
$t_{d(off)}$	Turn-Off Delay Time	—	51	—		
$t_f$	Fall Time	—	51	—		
$L_D$	Internal Drain Inductance	—	5.0	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	13	—		
$C_{iss}$	Input Capacitance	—	1300	—	pF	$V_{GS} = 0\text{V}$ $V_{DS} = -25\text{V}$ $f = 1.0\text{MHz}$ , See Fig. 5 ⑤
$C_{oss}$	Output Capacitance	—	400	—		
$C_{rss}$	Reverse Transfer Capacitance	—	240	—		

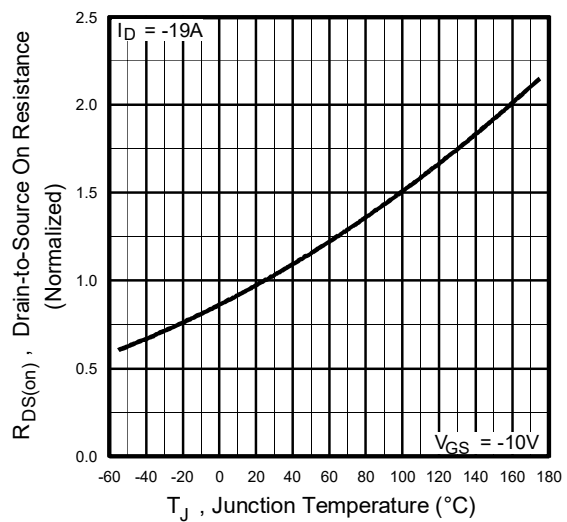
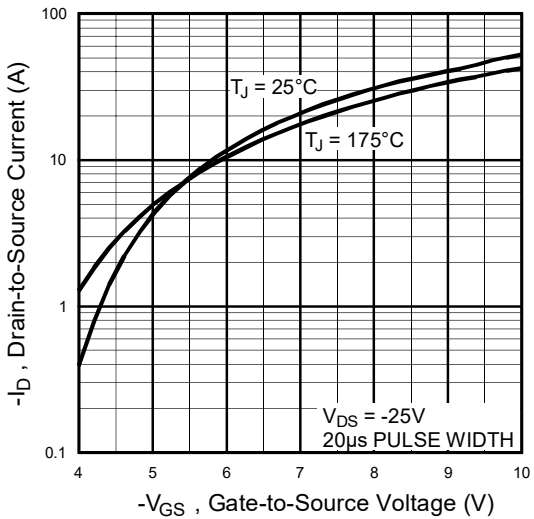
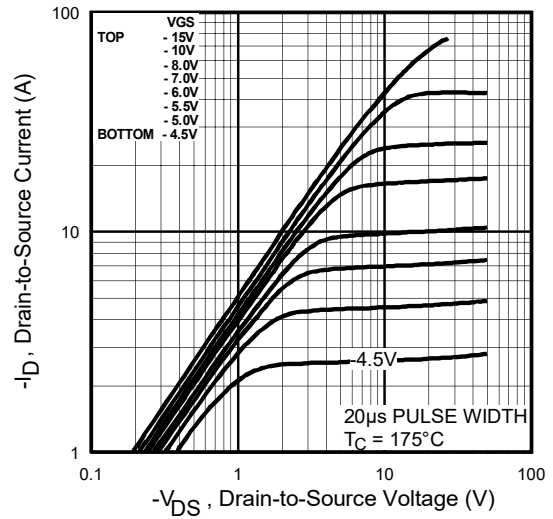
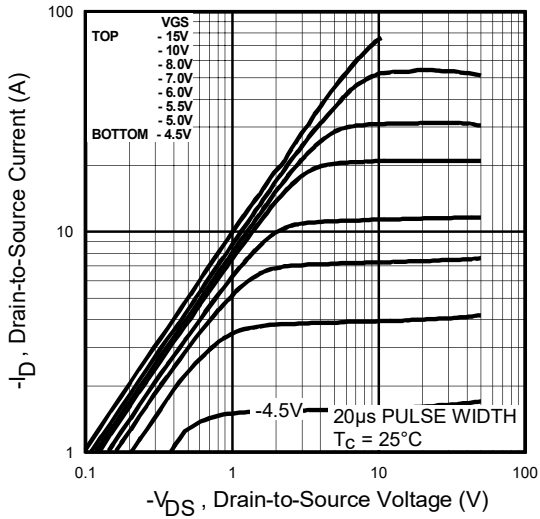


## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	-23	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ① ②	—	—	-76		
$V_{SD}$	Diode Forward Voltage	—	—	-1.3	V	$T_J = 25^\circ\text{C}$ , $I_S = -13\text{A}$ , $V_{GS} = 0\text{V}$ ④
$t_{rr}$	Reverse Recovery Time	—	150	220	ns	$T_J = 25^\circ\text{C}$ , $I_F = -11\text{A}$
$Q_{rr}$	Reverse Recovery Charge	—	830	1200	$\mu\text{C}$	$di/dt = -100\text{A}/\mu\text{s}$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

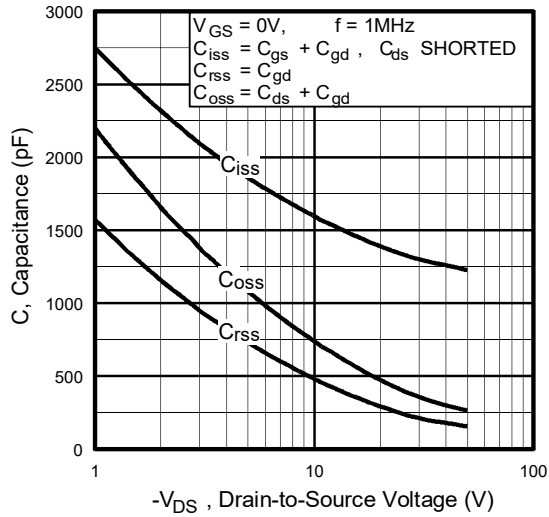
### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 7.1\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = -11\text{A}$ . (See Figure 12)
- ③  $I_{SD} \leq -11\text{A}$ ,  $di/dt \leq -470\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤ Uses IRF9540N data and test conditions

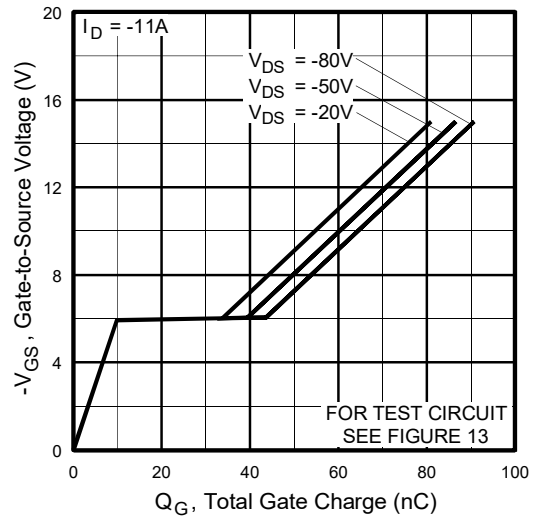


# IRFP9140NPbF

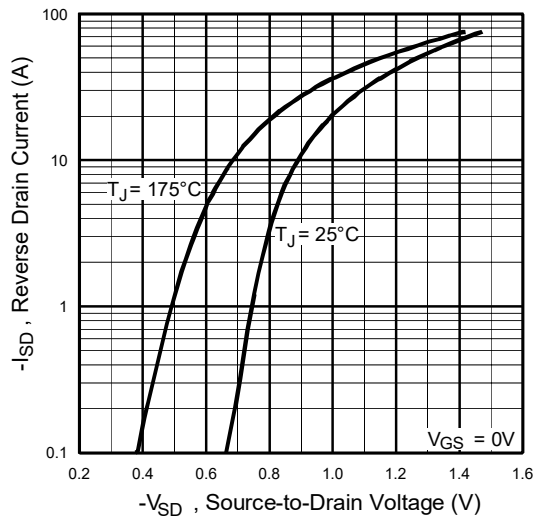
International  
**IGOR** Rectifier



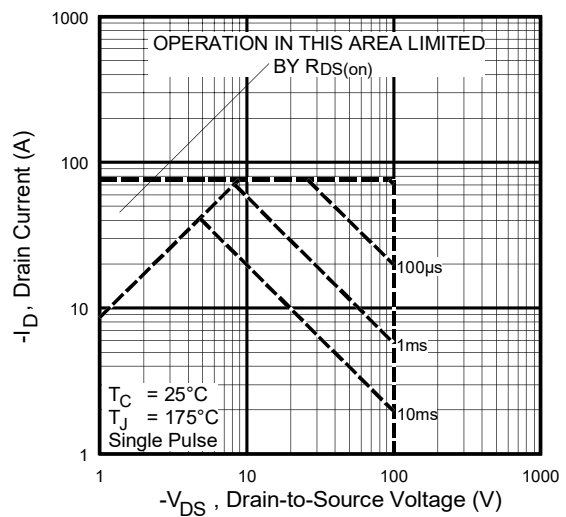
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



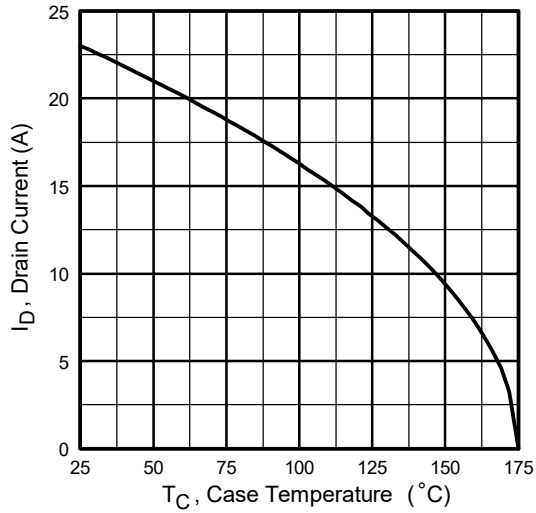
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



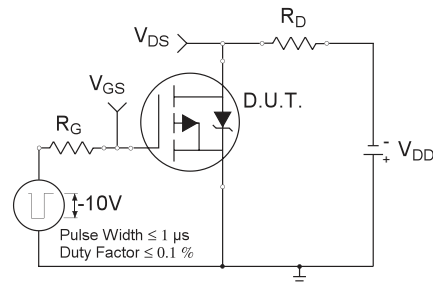
**Fig 7.** Typical Source-Drain Diode Forward Voltage



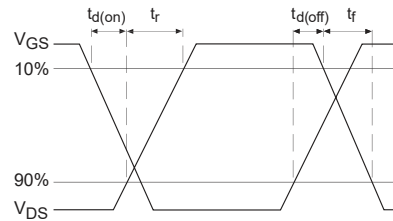
**Fig 8.** Maximum Safe Operating Area



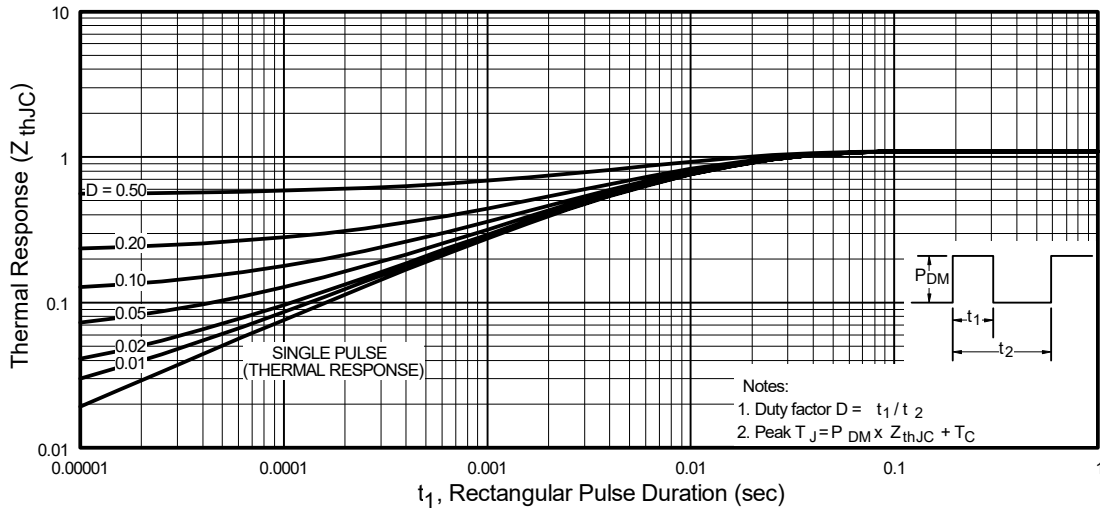
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



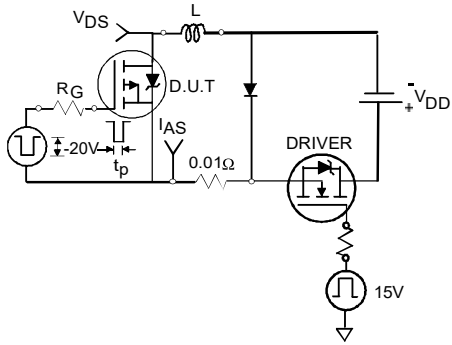
**Fig 10b.** Switching Time Waveforms



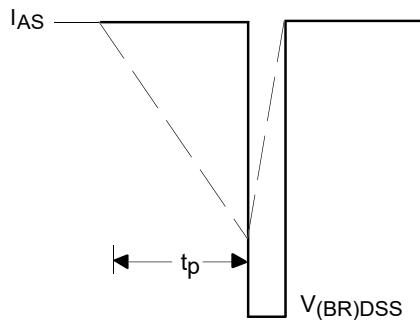
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

# IRFP9140NPbF

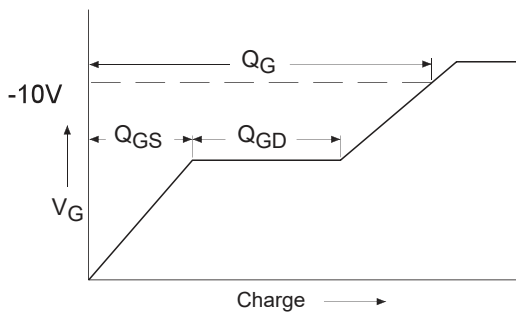
International  
**IGOR** Rectifier



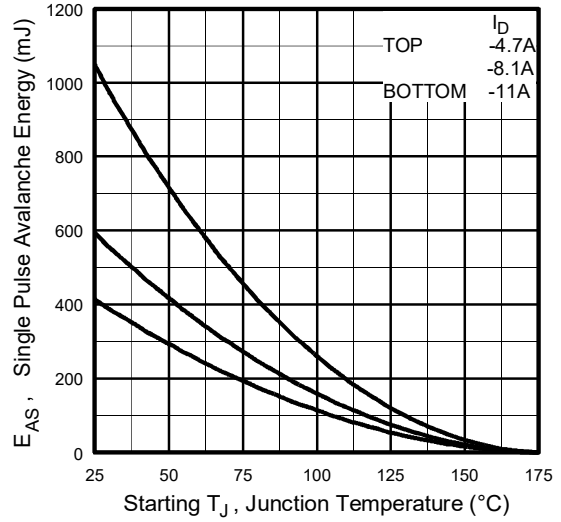
**Fig 12a.** Unclamped Inductive Test Circuit



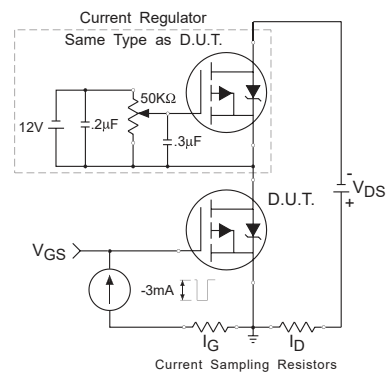
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

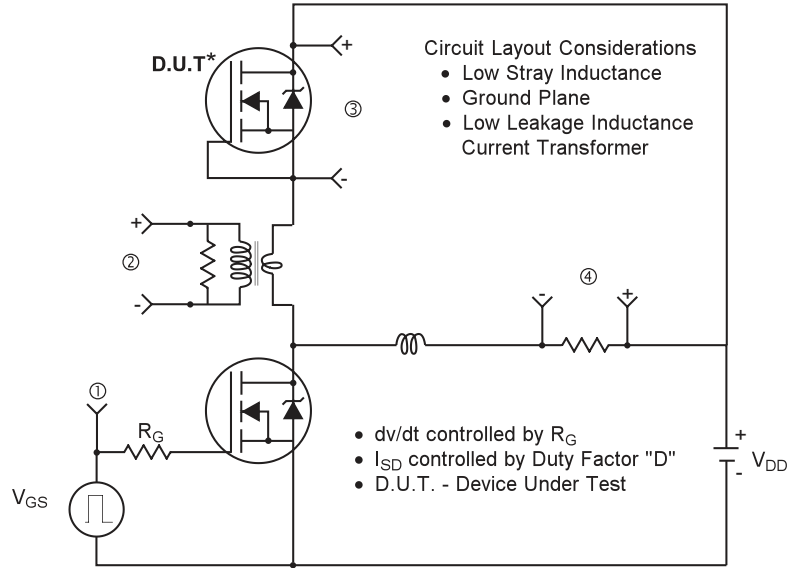


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

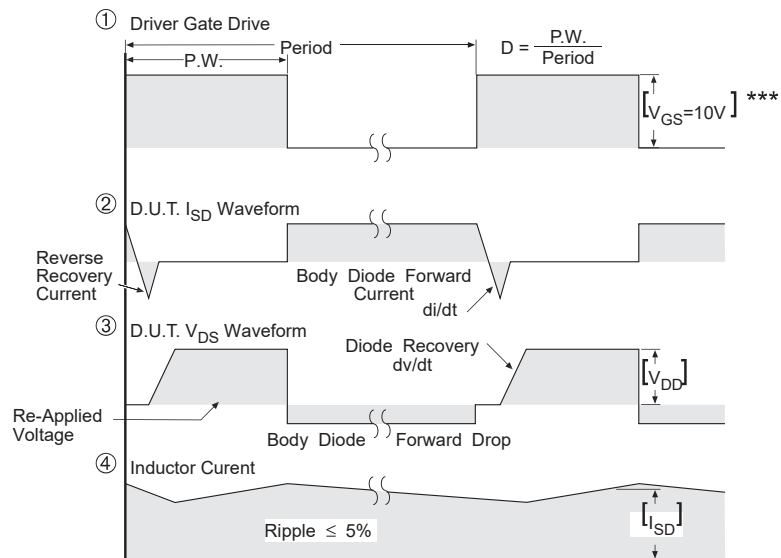


**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity of D.U.T for P-Channel



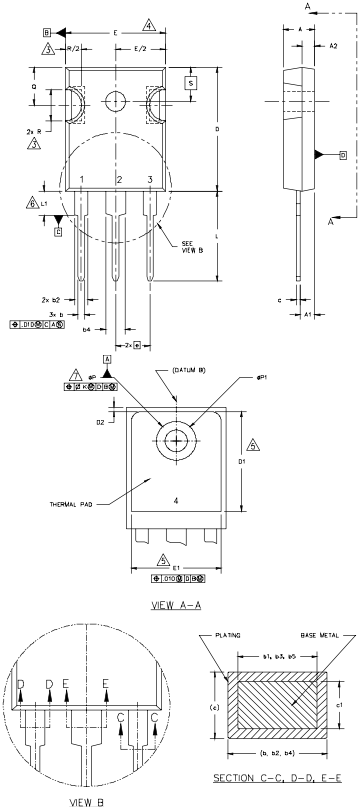
\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

**Fig 14.** For P-Channel HEXFETS

# IRFP9140NPbF



TO-247AC Package Outline Dimensions are shown in millimeters (inches)



NOTES:

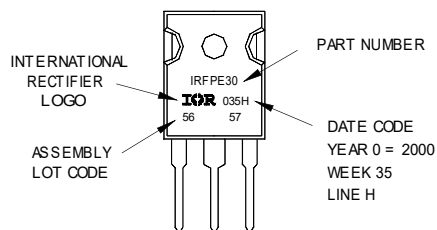
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
2. DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
3. CONTOUR OF SLOT OPTIONAL.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
6. LEAD FINISH UNCONTROLLED IN L1.
7.  $\phi P$  TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5° TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154" [3.91].
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247 WITH THE EXCEPTION OF DIMENSION c.

SYMBOL	DIMENSIONS				NOTES	LEAD ASSIGNMENTS
	INCHES		MILLIMETERS			
	MIN.	MAX.	MIN.	MAX.		
A	.183	.209	4.65	5.31		
A1	.087	.102	2.21	2.59		
A2	.059	.098	1.50	2.49		
b	.039	.055	0.99	1.40		HEXFET
b1	.039	.053	0.99	1.35		1.- GATE
b2	.065	.094	1.65	2.39		2.- DRAIN
b3	.065	.092	1.65	2.37		3.- SOURCE
b4	.102	.135	2.59	3.43		4.- DRAIN
b5	.102	.133	2.59	3.38		
c	.015	.034	0.38	0.86		
c1	.015	.030	0.38	0.76		IGBTs, CoPACK
D	.776	.815	19.71	20.70	4	
D1	.515	-	13.08	-	5	1.- GATE
D2	.020	.030	0.51	0.76		2.- COLLECTOR
E	.602	.625	15.29	15.87	4	3.- EMITTER
E1	.540	-	13.72	-		4.- COLLECTOR
e	.215 BSC		5.46 BSC			
Wk	.010		2.54			
L	.559	.634	14.20	16.10		DIODES
L1	.146	.169	3.71	4.29		1.- ANODE/OPEN
N	.3		7.62 BSC			2.- CATHODE
$\phi P$	.140	.144	3.56	3.66		3.- ANODE
$\phi P1$	-	.275	-	6.98		
Q	.209	.224	5.31	5.69		
R	.178	.216	4.52	5.49		
S	.217 BSC		5.51 BSC			

## TO-247AC Part Marking Information

EXAMPLE: THIS IS AN IRFPE30 WITH ASSEMBLY LOT CODE 5657 ASSEMBLED ON WW 35, 2000 IN THE ASSEMBLY LINE "H"

Note: "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.



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TAC Fax: (310) 252-7903

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Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>